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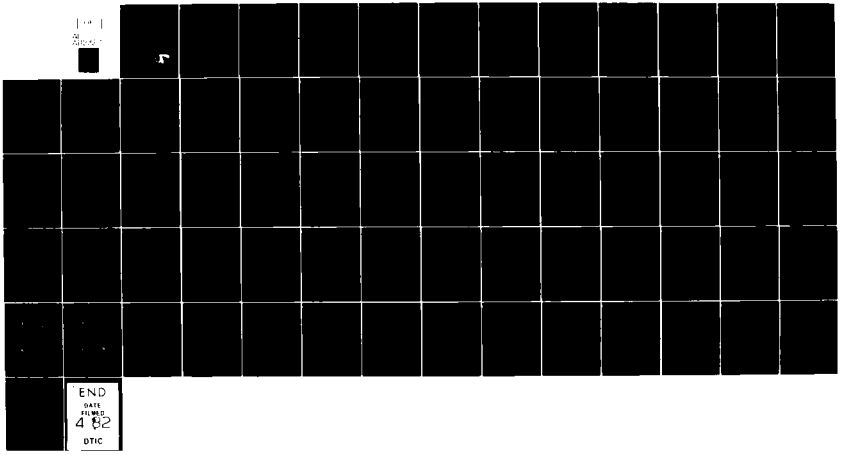

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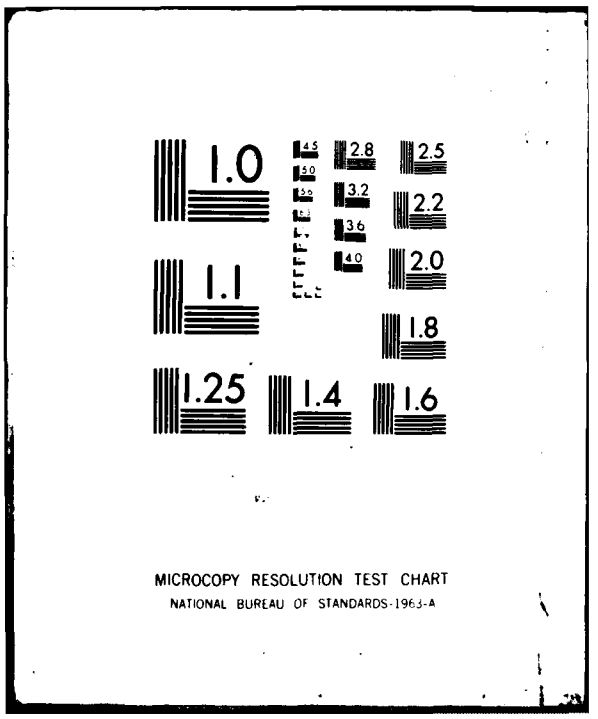
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AFATL-TR-81-37, Volume I

Effects of Sample Rates and Data Latency on Digital Autopilots

Volume I - Analysis Summary

A J Ventre
J F Meadows
W F Anderson, et al

COMPUTER SCIENCES CORPORATION
DEFENSE SYSTEMS DIVISION
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FINAL REPORT FOR PERIOD JANUARY 1980-DECEMBER 1980

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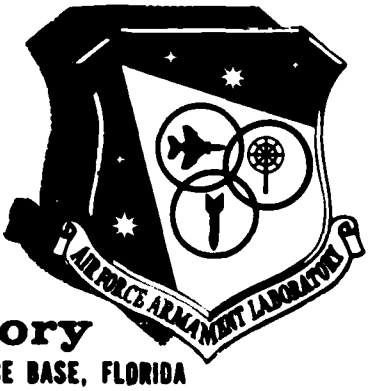

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

One of the objectives of the USAF Digital Integrating Subsystem (DIS) project is to establish standards for digitally interfacing various guidance options, seekers, autopilots, etc., in future air-to-air and air-to-surface tactical weapons. Since a DIS missile is digital in nature, time delays and related phase lags are present which affect system stability. This study is an attempt to address the data latency/stability problem.

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PREFACE

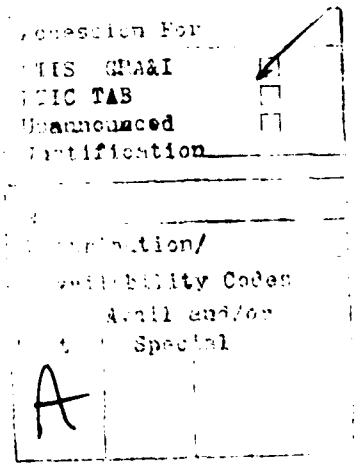
This two-volume report was prepared by the Defense Systems Division, Computer Sciences Corporation, 200 Sparkman Drive, Huntsville, Alabama 35807 under Contract No. F08635-77-C-0292, Task Order ADL-80-02 with the Air Force Armament Laboratory, Armament Division, Eglin Air Force Base, Florida 32542. Dr. J. W. Jones (DLMM) monitored the program for the Armament Laboratory. This effort was conducted during the period from January 1980 to December 1980. This is Volume I.

The Public Affairs Office has reviewed this report, and it is releasable to the National Technical Information Service, where it will be available to the general public, including foreign nationals.

This report has been reviewed and is approved for publication.

FOR THE COMMANDER

PETER D. TANNEN, Colonel, USAF
Chief, Guided Weapons Division



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LIST OF ILLUSTRATIONS (CONCLUDED)

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NOMENCLATURE

ACK	Acknowledge
BIU	Bus Interface Unit
CPU	Central Processing Unit
CSC	Computer Sciences Corporation
DAP	Digital Autopilot
DIS	Digital Integrating Subsystem
DISMUX	DIS Multiplex
DMA	Direct Memory Access
FCAS	Flight Control Actuation Subsystem
GBU	Glide Bomb Unit
GFE	Government Furnished Equipment
ILAAT	Inter-Laboratory Air-to-Air Technology
I/O	Input/Output
IOC	Input/Output Controller
K_I	Adaptive Gain
K_V	Autopilot Rate Loop Gain Yaw
$K_{\dot{\lambda}_p}$	Roll Homing Loop Gain
LCIGS	Low Cost Inertial Guidance Subsystem
LOS	Line-of-Sight
PIO	Parallel Input/Output
RRPP	Round Robin Passing Protocal
SIO	Serial Input/Output
T	Sampling Period
XMIT	Transmit
$\dot{\lambda}_r$	Yaw Line-of-Sight Rate
$\dot{\lambda}_q$	Pitch Line-of-Sight Rate
ω_d	DAP Dither Frequency

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SECTION I
INTRODUCTION

1.1 PURPOSE OF THE DATA LATENCY STUDY

One of the objectives of the USAF Digital Integrating Subsystem (DIS) project is to establish methodologies for digitally integrating various guidance options, seekers, fuzes, autopilots, etc., in future air-to-surface and air-to-air tactical weapons. One of the characteristics of the DIS scheme is flexibility in interconnecting the processors with various subsystems through a variety of input/output (I/O) interfaces. Because of this flexibility, there is considerable latitude in interfacing the digital autopilot with the inertial measurement data, guidance commands, and actuator commands. However, the interprocessor data transfer introduces time delays. Time shared buses such as the DISMUX (DIS time division multiplex bus with round-robin passing protocol) introduce additional and variable access latency. The effect of this delay/latency on the stability/performance of a missile depends on the magnitude of the delays, the control system dynamics, and sample rates. The purpose of this study is to examine the latency inherent in DIS interprocessor communication schemes, especially in the Low Cost Inertial Guidance Subsystem (LCIGS), the Flight Control Actuation Subsystem (FCAS) and the Digital Autopilot (DAP) and to obtain quantitative data relating missile performance to time delay.

1.2 SCOPE OF THIS REPORT

This report (Volume I) is presented in five sections. Section I defines the overall objectives of the study. The DIS subsystem architecture, interprocessor communication schemes and variable latency phenomena are discussed in Section II. The relationship between data latency and system stability is presented in Section III together with mathematical models of two typical missile systems which might employ a DIS-like subsystem. Analyses of the mathematical models are discussed in

Section IV together with simulation results. Concluding comments are made in Section V.

Volume II of this report is the software guide.

SECTION II

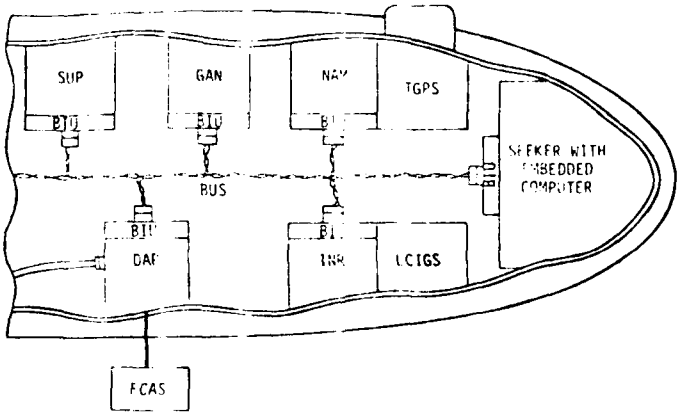
DIGITAL INTEGRATION SUBSYSTEM INTERPROCESSOR COMMUNICATION SCHEMES

2.1 GENERAL

In the next two parts of this section, the DIS subsystem architecture and three static latency interprocessor communication schemes associated with that architecture are discussed. In the last two parts of this section, the variable data latencies associated with those communication schemes are analyzed and a recommended data transfer methodology is presented.

2.2 DIS SUBSYSTEM ARCHITECTURE

A general DIS architectural scheme is shown in Figure 1 (Ref. 1). A discussion of the functions of each of the modules shown in Figure 1 can be found in References 2 through 5. The three modules addressed in this study are the LCIGS, the DAP, and the FCAS. Each is digital processor based and is discussed more fully in the following paragraphs.



NOTE:
SUP - SUPERVISOR
GAN - GUIDANCE AND NAVIGATION
NAV - NAVIGATION AIMING MANAGEMENT
TGPS - TACTICAL GLOBAL POSITIONING SYSTEM
DAP - DIGITAL AUTOPILOT
INR - INERTIAL NAVIGATION
LCIGS - LOW COST INERTIAL GUIDANCE SYSTEM
BIU - BUS INTERFACE UNIT
FCAS - FLIGHT CONTROL ACTUATION SYSTEM

Figure 1. General DIS Architectural Scheme (Ref. 1)

2.2.1 LCIGS – LOW COST INERTIAL GUIDANCE SUBSYSTEM

LCIGS is a digitally based, strapdown inertial sensor. It contains three accelerometers and three rate-integrating gyros. These instruments sense the missile longitudinal and lateral accelerations and attitude rates. The LCIGS computer processes these sensor outputs and produces missile body incremental velocity and attitude information (Figure 2). The LCIGS output is used by the autopilot for vehicle stabilization and closed loop steering control.

LCIGS consists of three sets (orthogonal) of five functional units shown in detail in Figure 3. The Gyro Sensor Electronics Unit senses roll, pitch and yaw motion and is interconnected by the Gyro Torquer Electronics Unit to the Gyro Processor Unit. It is the task of each gyro processor unit (there are three of them) to provide gyro loop control by sending gyro torque rebalance commands to the Gyro Torquer Electronics Unit. Accumulated angular commands are sent to the Service Processor Unit by the Gyro Processor Unit together with the output from the Accelerometer Electronics Unit. The accelerometers are pendulous type with pulse-rebalance closed loop control. The output pulse rate is proportional to acceleration. Each individual pulse represents a velocity increment. The incremental velocity pulses are accumulated by a counter over a period of 2.5 (10^{-3}) sec and then sent to the Service Processor Unit. The Service Processor Unit then sends the accelerometer velocity and gyro angular data to the autopilot. A more complete description of the LCIGS can be found in Reference 5.

2.2.2 DAP – DIGITAL AUTOPILOT

The autopilot provides the mechanism to close the loop between the sensed angular rates from the LCIGS and the actuator motors (FCAS) of the missile control surfaces (fins) to aerodynamically stabilize the vehicle (Ref. 3).

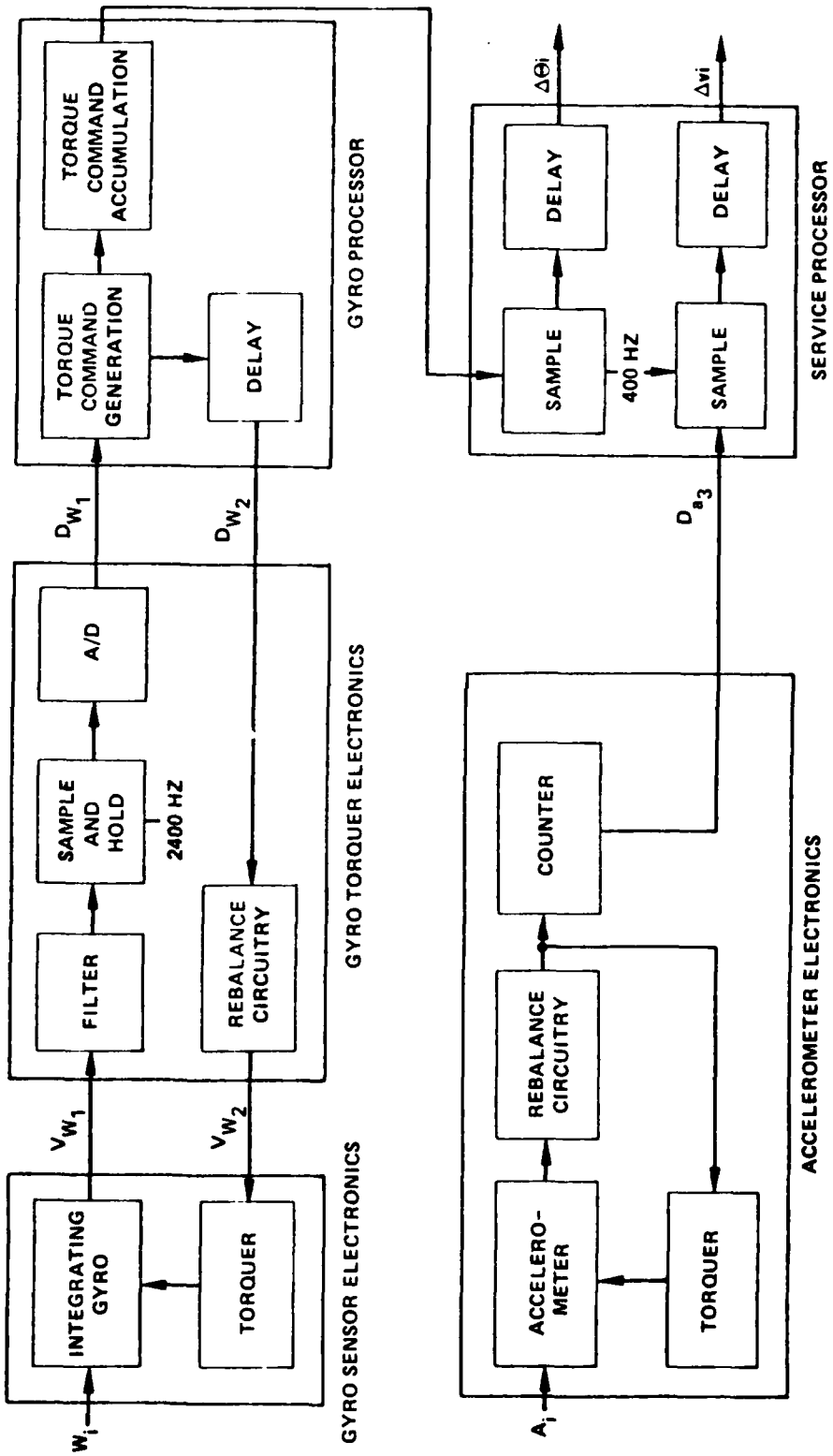


Figure 2. Low Cost Inertial Guidance Subsystem Block Diagram

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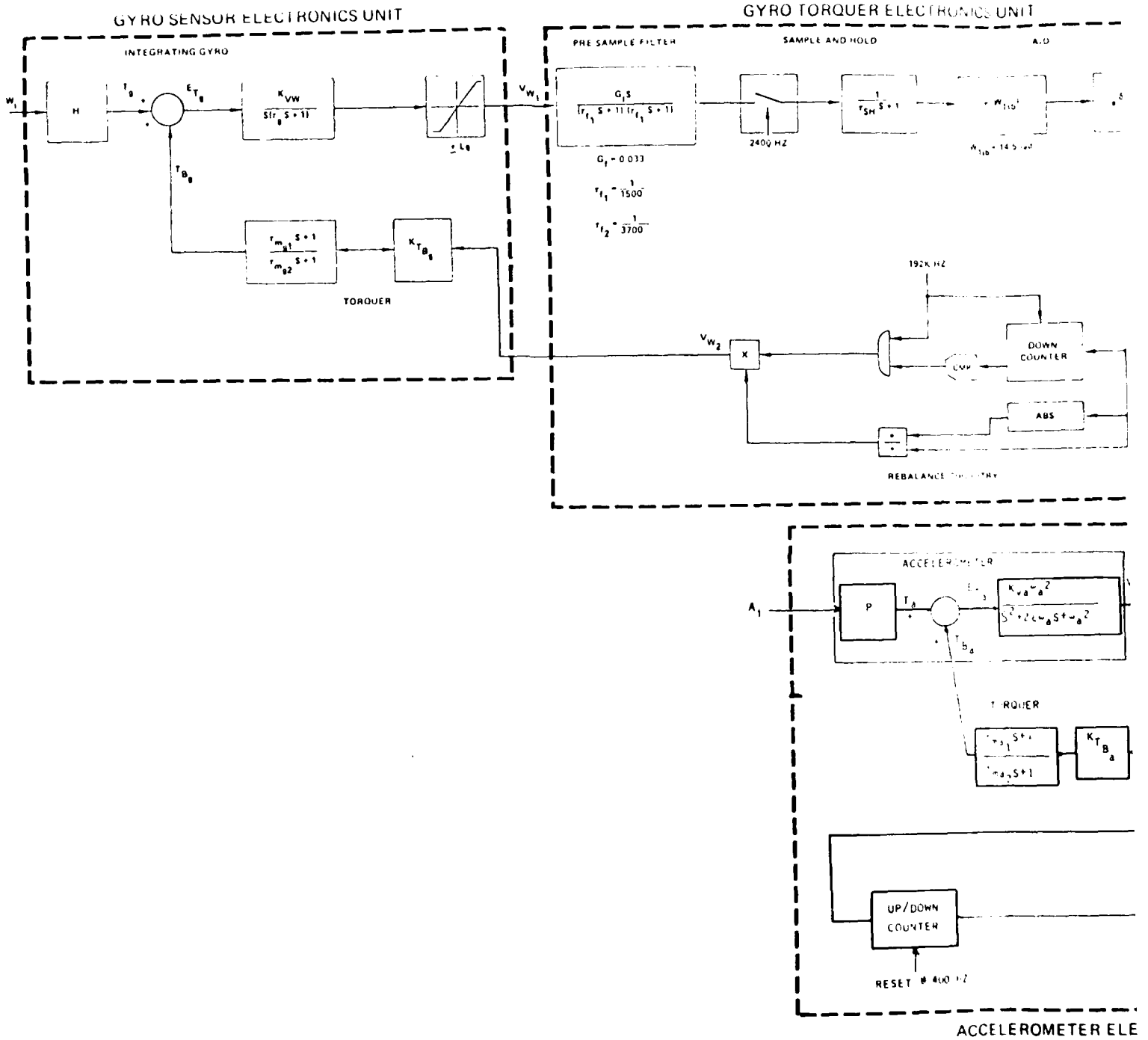
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INTEGRATING GYRO
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TORQUER
GYRO TORQUER ELECTRONICS UNIT
PRE SAMPLE FILTER
SAMPLE AND HOLD
A/D
2400 HZ
192K HZ
DOWN COUNTER
ABS
ACCELEROMETER
P
TORQUER
UP/DOWN COUNTER
RESET @ 400 HZ
ACCELEROMETER ELE

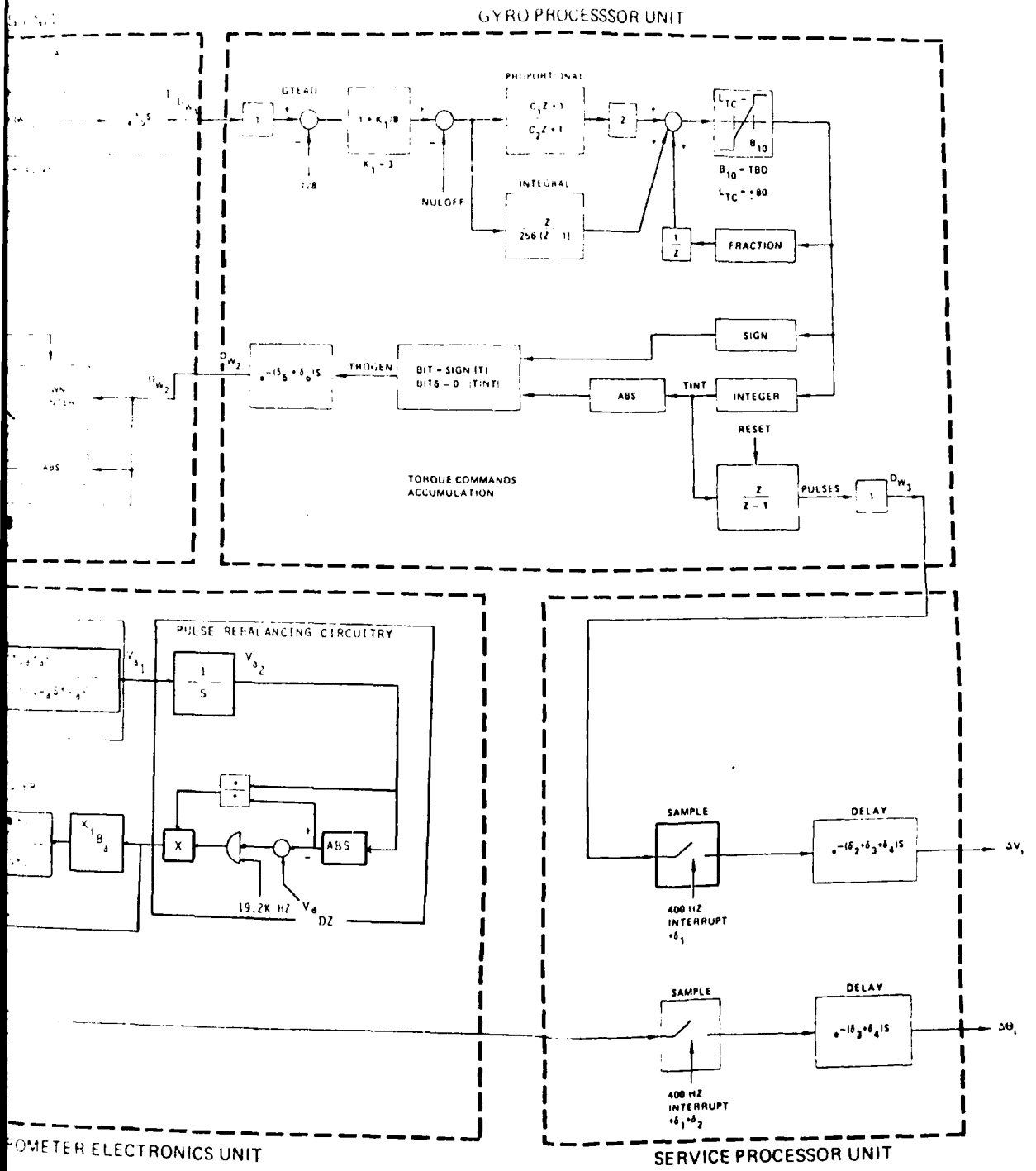

Figure 3. Detailed LCIGS Block Diagram

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The miniaturization, availability, and low cost of digital hardware have made it possible to construct digital autopilots whose performance is comparable to or exceeds that of analog autopilots. The digital autopilot allows for extensive trajectory shaping, variable parameter filters, scheduled gains, and other complex control techniques which would be difficult if not impossible to implement with analog autopilots (Ref. 6). A block diagram of a typical missile digital autopilot is shown in Figure 4. Note that the filters are digital in nature and as such contain a sampling parameter "T" (also called the sampling time). The sample rate (1/T) associated with any digital autopilot is missile design-dependent. The transport lag associated with calculation time delays is a critical aspect of the digital autopilot operation and will be discussed in more detail below.

2.2.3 FCAS – FLIGHT CONTROL ACTUATION SUBSYSTEM

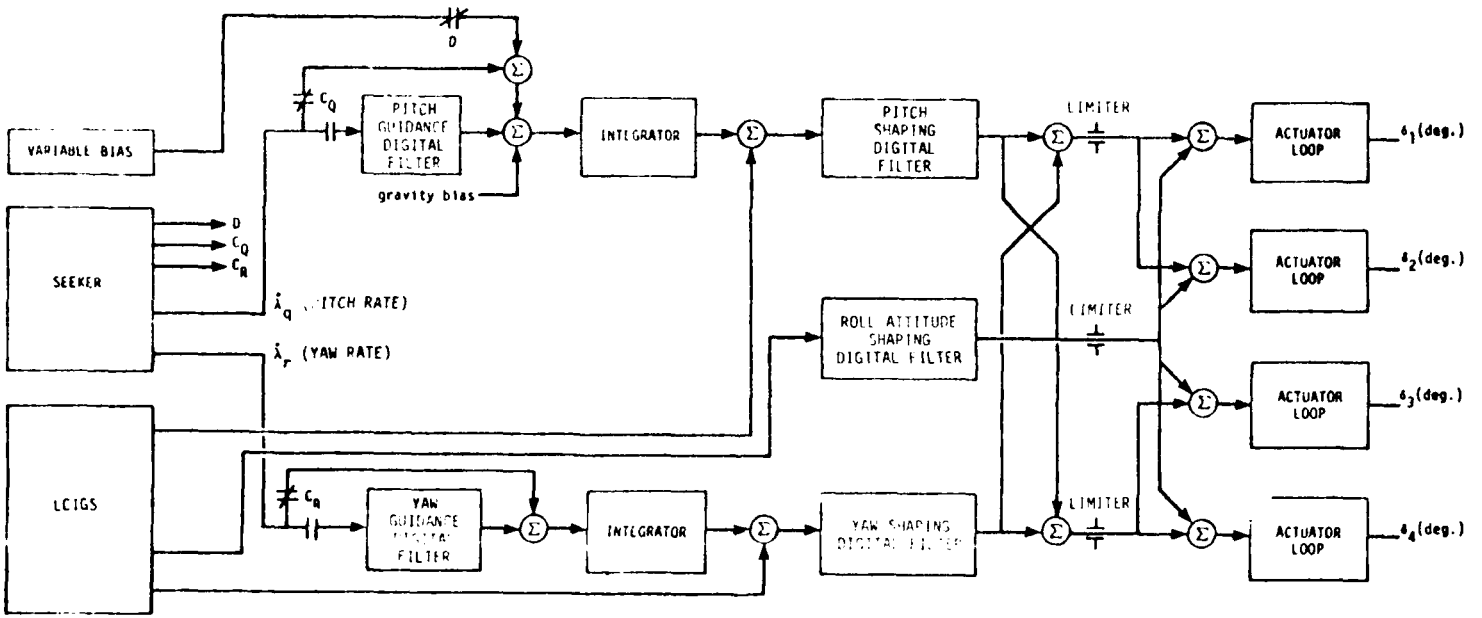
The purpose of the FCAS is to deflect the missile fins in response to commands from the autopilot. The fins may be electrically, pneumatically, or hydraulically actuated depending on the design of the FCAS and missile mission.

A block diagram representation of a typical FCAS is shown in Figure 5.

2.3 DIS STATIC LATENCY INTERPROCESSOR COMMUNICATION SCHEMES

Data flow (I/O) between the previously discussed subsystems are in digital form and can be any of several types: SIO (Serial Input/Output), PIO (Parallel Input/Output), or by DISMUX (DIS Multiplex) bus. Latency time is a function of the execution times of each subsystem processor and is dependent upon the interprocessor I/O configuration.

The following paragraphs contain a preliminary assessment of the LCIGS/DAP static latencies associated with the three interprocessor communication schemes mentioned above. A variable latency analysis appears in Paragraph 2.4.



C_Q = signal crossover in pitch channel
C_R = signal crossover in yaw channel
D = true track

Figure 4. Typical Digital Autopilot Block Diagram

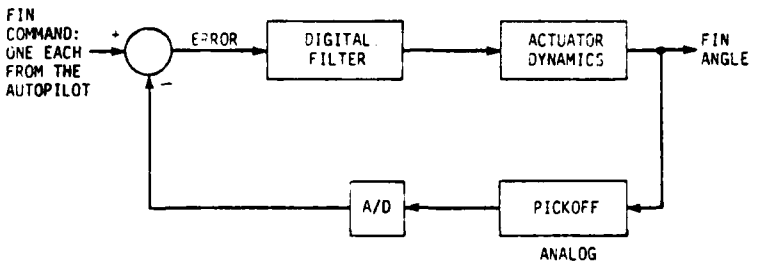


Figure 5. Typical FCAS Block Diagram (Ref. 6)

2.3.1 DISMUX Bus I/O

Bus access for a particular computer is controlled by a Bus Interface Unit (BIU). The BIU contains a one word buffer which can communicate directly with its host computer (processor) via a direct memory access (DMA) channel.

Interprocessor data transmission between the LCIGS and DAP via the DISMUX bus is shown schematically in Figure 6. The processor sets a transmit enable control bit when it has a message to transmit. When bus access is granted, the LCIGS data is transferred from memory to the BIU and then transmitted to the DAP BIU. The DAP BIU stores the message in memory as it is received. Table 1 lists the significant events and times associated with LCIGS/DAP data communication over the DISMUX bus. The entry under "WAIT FOR BUS ACCESS" is nominal data taken from Reference 7. A detailed simulation of the DIS bus traffic is presented in Volume II and discussed in more detail in Appendix B.

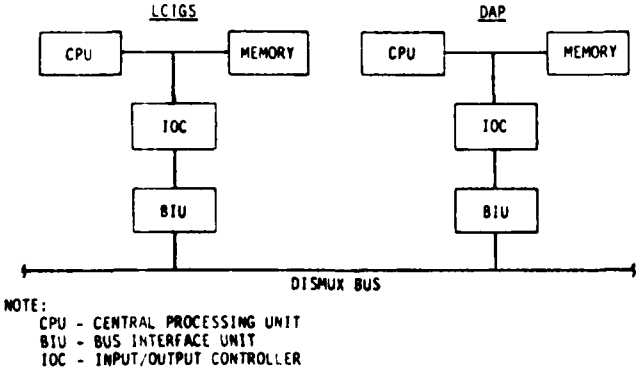


Figure 6. DIS Processor Interconnections Via DISMUX Bus

TABLE 1. LCIGS/DAP COMPUTER AND DISMUX BUS SIGNIFICANT EVENT TIMES

EVENT	TIME (10^{-3} sec)
SENDING COMPUTER (LCIGS)	
(a) MAIN MEMORY I/O INTERRUPT	0.001
(b) DATA TRANSFER SET-UP	0.096
(c) DATA TRANSFER ENABLE	0.002
(d) LOAD BIU MEMORY	0.012
(e) WAIT FOR BUS ACCESS (REF. 7)	0.199
(f) SEND I/O ENABLE INTERRUPT TO DAP	0.002
(g) WAIT FOR DAP ACK (SERVICE PROCESSOR ROUTINE)	0.145
(h) WAIT FOR BUS ACCESS (REF. 7)	0.199
(i) DISMUX MESSAGE TRANSFER	0.187
	0.843
RECEIVING COMPUTER (DAP)	
(a) DISMUX MESSAGE RECEIVED (EOT)	0.002
(b) BIU/MAIN MEMORY I/O REQUEST	0.001
(c) DATA TRANSFER SET-UP (FROM BIU)	0.096
(d) DATA TRANSFER ENABLE	0.002
(e) LOAD MEMORY	0.012
	0.113
TOTAL	0.956

NOTE:

1) ALL TIMES ARE ESTIMATES.
2) MESSAGE LENGTH OF 9 WORDS ASSUMED (INCLUDES 2 COMMAND WORDS) [BOM, EOT]
3) INTERNAL TRANSFER RATE OF 0.002 (10^{-3}) SEC/WORD IS ASSUMED

2.3.2 Serial Data Transfer

Serial data transfer between processors is accomplished using a dedicated hardware link between processors. An IOC and a serial I/O card containing a 16-bit shift register are used to effect bit-by-bit data transfer between processors. Assume the LCIGS is the sending computer and the DAP the receiving computer. When the LCIGS is ready to send its attitude and velocity

data to the DAP, an I/O ENABLE interrupt is sent by the LCIGS processor to the DAP. When sensed by the DAP processor, an internal interrupt is generated and an I/O service routine is called. The DAP processor sends an ACK to the LCIGS processor acknowledging the interrupt and prepares to receive the LCIGS message (data). The LCIGS sends the message to the DAP SIO shift register, bit-by-bit until the information transfer is complete. The DAP processor then empties the contents of the shift register into memory. The significant events and times associated with serial data transfer between the LCIGS and DAP are shown in Table 2.

TABLE 2. LCIGS/DAP COMPUTER AND SERIAL I/O SIGNIFICANT EVENT TIMES

EVENT	TIME (10^{-3} sec)
SENDING COMPUTER (LCIGS)	
(a) MEMORY I/O INTERRUPT	0.001
(b) SHIFT REGISTER DATA TRANSFER SET-UP	0.046
(c) DATA TRANSFER ENABLE	0.002
(d) LOAD SHIFT REGISTERS	0.012
(e) SEND I/O ENABLE INTERRUPT TO DAP	0.002
(f) WAIT FOR DAP ACK (SERVICE PROCESSOR ROUTINE)	0.145
(g) SERIAL DATA MESSAGE TRANSFER (BIT-BY-BIT)	0.220
	0.428
RECEIVING COMPUTER (DAP)	
(a) SERIAL DATA MESSAGE RECEIVED (EOT)	0.002
(b) SHIFT REGISTER/MEMORY I/O REQUEST	0.001
(c) DATA TRANSFER SET-UP	0.046
(d) DATA TRANSFER ENABLE	0.002
(e) LOAD MEMORY	0.012
	0.063
TOTAL	0.491

NOTE:
1) ALL TIMES ARE ESTIMATES
2) MESSAGE LENGTH OF 9 WORDS ASSUMED (INCLUDES 2 COMMAND WORDS)
3) DATA ENTERS SHIFT REGISTERS FROM CORE MEMORY IN PARALLEL
4) SHIFT REGISTER LOAD TIME IS 0.002 (10^{-3}) SEC/WORD*7 DATA WORDS

2.3.3 Parallel Data Transfer

Parallel data transfer is accomplished using a dedicated hardware link where whole words (16 bits each) are transferred with a single clock pulse. The transmitting and receiving processors (e.g., LCIGS and DAP, respectively) are connected via IOC and parallel I/O cards. Each parallel I/O card contains two buffer areas of 16 bits each, one for input and one for output.

The I/O events which occur during interprocessor communication are very similar to those which occur during serial data transfer except that 16 bits are sent with each clock pulse instead of one bit at a time.

The significant events and times associated with parallel data transfer between the LCIGS and DAP are shown in Table 3.

TABLE 3. LCIGS/DAP COMPUTER AND PARALLEL I/O SIGNIFICANT EVENT TIMES

EVENT	TIME (10^{-3} sec)
SENDING COMPUTER (LCIGS)	
(a) MEMORY I/O INTERRUPT	0.001
(b) SHIFT REGISTER DATA TRANSFER SET-UP	0.046
(c) DATA TRANSFER ENABLE	0.002
(d) LOAD PARALLEL REGISTERS	0.012
(e) SEND I/O ENABLE INTERRUPT TO DAP	0.002
(f) WAIT FOR DAP ACK	0.145
(g) PARALLEL DATA MESSAGE TRANSFER (AVERAGE) (WORD-BY-WORD)	0.017
	0.225
RECEIVING COMPUTER (DAP)	
(a) PARALLEL DATA MESSAGE RECEIVED	0.002
(b) REGISTER/MEMORY I/O REQUEST	0.001
(c) DATA TRANSFER SET-UP	0.046
(d) DATA TRANSFER ENABLE	0.002
(e) LOAD MEMORY	0.012
	0.063
TOTAL	0.288

NOTE:

1) ALL TIMES ARE ESTIMATES
2) MESSAGE LENGTH OF 9 WORDS ASSUMED (INCLUDES 2 COMMAND WORDS)
3) SHIFT REGISTER LOAD TIME IS 0.002 (10^{-3}) SEC/WORD*7 DATA WORDS

2.3.4 Summary

A preliminary assessment of the significant event times associated with LCIGS/DAP data communications is given in Tables 1, 2, and 3. A summary of the total event times is presented in Table 4. It is apparent that parallel data communication between two processors takes less time than serial I/O or DISMUX bus data communication and is the preferred method of transmitting time-critical data between the LCIGS and DAP if the only objective is to minimize time delay.

TABLE 4. PRELIMINARY ASSESSMENT OF LCIGS/DAP INTERPROCESSOR COMMUNICATION SCHEMES

SCHEME	TOTAL EVENT TIME (10^{-3} sec)
DISMUX BUS	0.956
SERIAL I/O	0.491
PARALLEL I/O	0.288

A more detailed evaluation of DIS interprocessor communication schemes is presented in the following paragraph where other DIS computer and I/O configurations are considered. The influence of additional DIS processors and interconnections on the data flow between the LCIGS-DAP-FCAS is examined.

2.4 DIS VARIABLE LATENCY ANALYSIS

The primary contributors to variable data latency are processor execution time, bus wait, data transmission, and asynchronous wait (Figure 7). Note in Figure 7 that the asynchronous wait is due to the aperiodic overlap of processor functions. These are dynamic processes which are functions of time and not static processes as discussed in Paragraph 2.3.

The results of an evaluation of the variable latency associated with the DIS LCIGS-DAP-FCAS interprocessor communication schemes (Appendix B) shown in Figure 8 are presented in Table 5. Note that Case A, the all parallel scheme, has the lowest latency time and will introduce the least amount of phase lag into a DIS missile system.

LATENCY CONTRIBUTORS

- ASYNCHRONOUS WAIT
- PROCESSOR EXECUTION
- DATA TRANSMISSION AND BUS WAITS

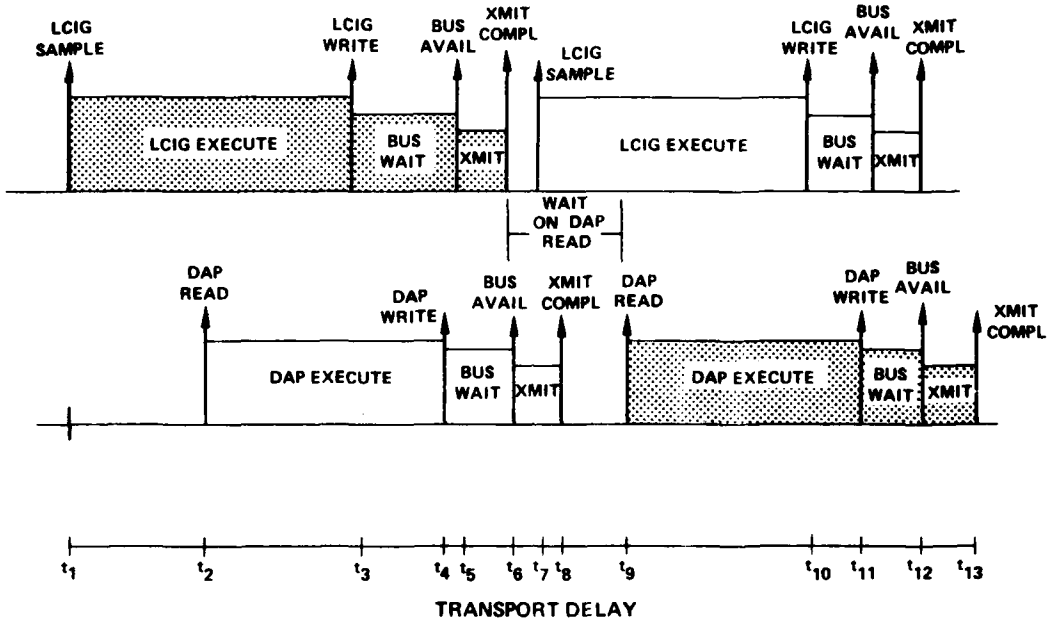


Figure 7. DIS Variable Data Latency Contributors

TABLE 5. DIS VARIABLE DATA LATENCY MODEL SIMULATION RESULTS

CASE	PROCESSOR EXECUTION TIME (SEC x 10^{-3})		BUS WAIT TIME (SEC x 10^{-3})	DATA XMIT TIME (SEC x 10^{-3})	ASYNCHRONOUS WAIT (SEC x 10^{-3})	TOTAL LATENCY (SEC x 10^{-3})
	LCIGS	DAP				
A	1.351	2.000	0.0	0.449	0.0	3.800
B	1.351	2.000	0.0	0.543	0.0	3.894
C	1.351	2.000	0.274	0.423	0.750	4.798
D	1.351	2.000	0.274	0.517	1.459	5.601
E	1.351	2.000	0.320	0.377	2.094	6.142

The model which simulates the DIS processor functions and their interconnections is presented in Volume II, Section II.

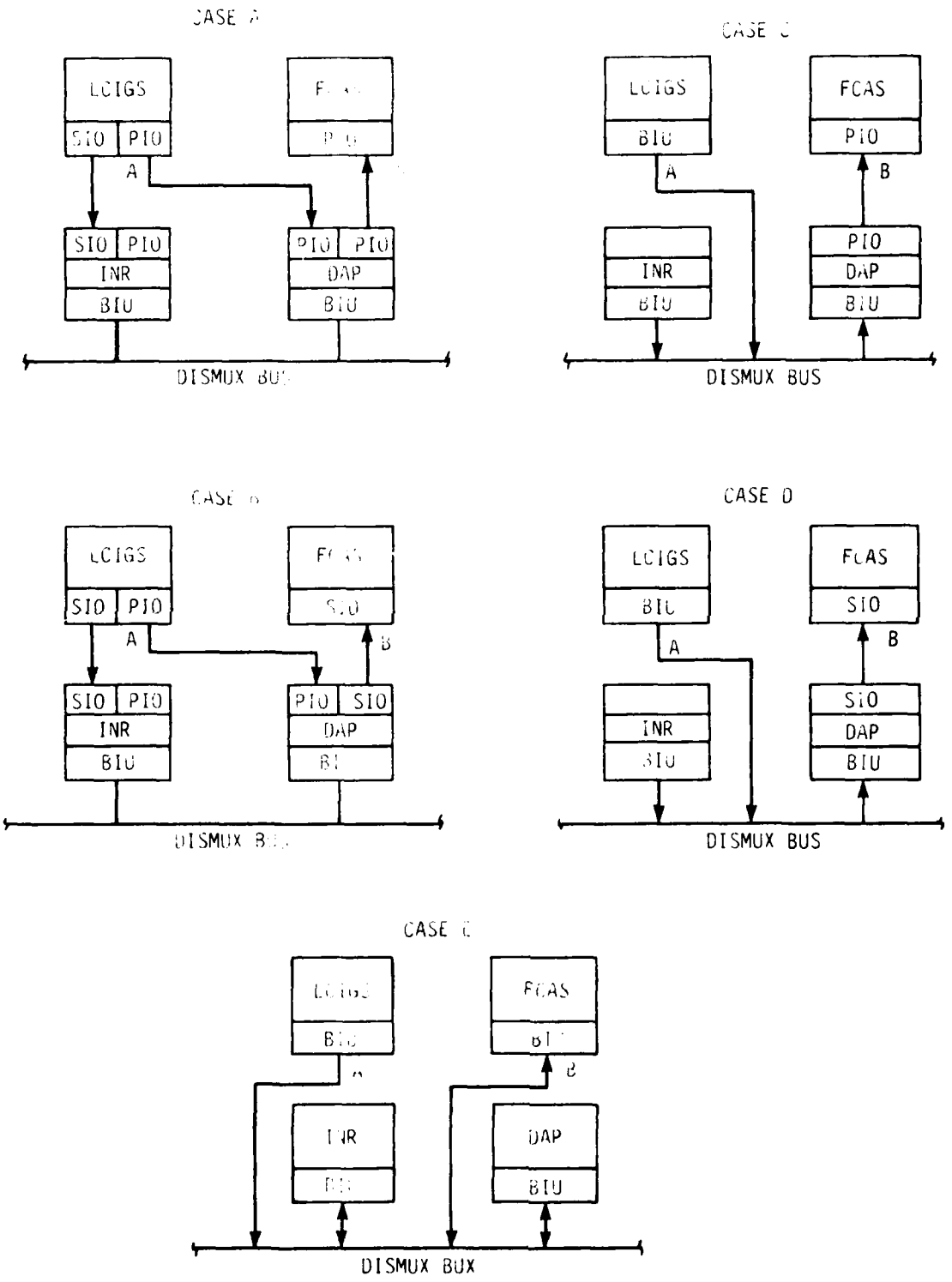


Figure 8. DIS Processor Interconnect Schemes

SECTION III
DATA LATENCY AND SYSTEM STABILITY

3.1 GENERAL

The nature of DIS static and variable latencies were discussed in Section II where it was demonstrated that the parallel interprocessor connection scheme introduced the least amount of time delay (hence phase lag) into the missile system. The need to minimize phase lag in missile systems is critical because missile stability and controllability are adversely affected by it.

The relationship between DIS data latency and missile system stability are briefly discussed in Paragraph 3.2 together with the stability analysis methodology used in this study.

Mathematical models of the selected air-to-air and air-to-surface missiles are presented in Paragraph 3.3. These models together with conventional frequency and time domain stability analysis tools are used in Section IV to predict missile system performance when data latencies are present.

3.2 STABILITY ANALYSIS METHODOLOGY

The relationship between the DIS processors and missile vehicle stability is shown in Figure 9. The data transport delay among the DIS processors causes a phase lag in the vehicle control loop which affects the missile system phase margin. When the phase margin falls below 45 degrees, system stability is considered to be unsatisfactory. A purpose of this study is to determine how much time delay (phase lag) the selected systems can sustain before becoming "unstable" or at least unsatisfactory.

To study the data latency/stability phenomena, mathematical models representing the DIS/missile vehicle control loop were developed and connected together as shown in Figure 9(B). Time delays representing data latency were inserted at points B and E

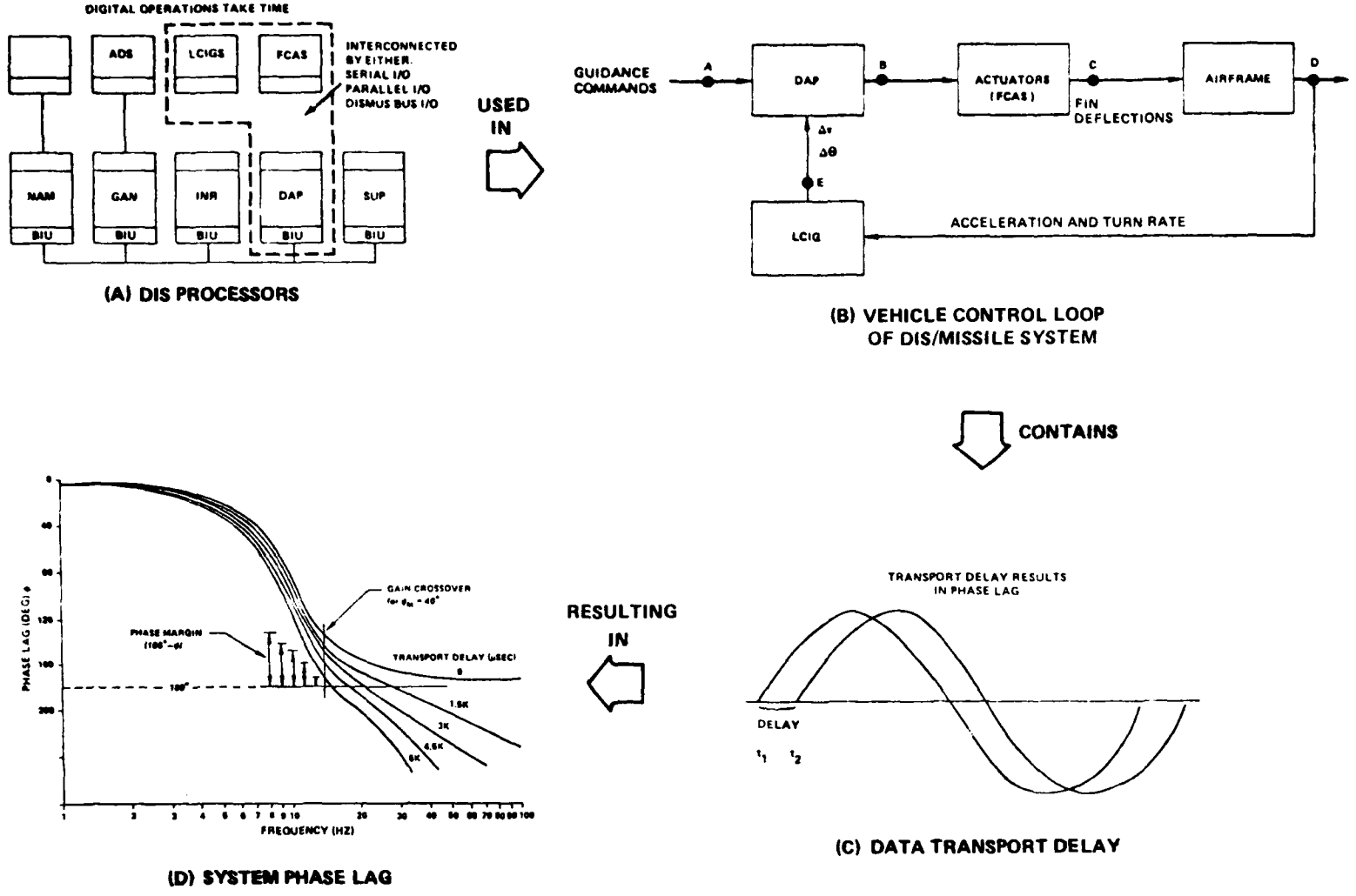


Figure 9. The Transport Delay Inherent In DIS/Missile Systems Causes Phase Lag Which Affects Missile Stability

in Figure 9(B) and are represented as phase shifts. The DIS/missile mathematical models discussed below were analyzed for stability using Bode magnitude and phase plots and time domain simulation (Ref. 8-11). In Section IV, frequency domain results are compared with time domain digital simulation results.

A discussion of the DIS/missiles used in the study is presented in the following paragraph.

3.3 MATHEMATICAL MODELS

To study the effects of data latency on missile system performance, a missile system must be selected and a DIS-like architecture configured for it. Two selected for this analysis are the Interlaboratory Air-to-Air Technology (ILAAT) missile model (Ref. 12) and the GBU-15 Planar Wing Weapon (Ref. 13). The former is a model of a high performance air-to-air missile and the latter is an air-to-surface guided bomb. These were chosen because of the availability of digital simulations for these missiles. Mathematical models of the DIS/ILAAT and GBU-15 are presented in the following paragraph.

3.3.1 ILAAT

The ILAAT missile is conceptual in nature and its purpose is to provide an integrated, full spectrum technology base for future tactical air-to-air missiles (Ref. 14). The bank-to-turn steering mechanism (autopilot) for maneuvering the ILAAT missile allows an unsymmetrical airframe design to be used with greater efficiency than conventional cruciform configurations (Ref. 15). ILAAT's high aerodynamic efficiency (large lift-to-drag ratio) and substantial load factor capability result in increased missile maneuvering performance. A more detailed description of the ILAAT missile can be found in Reference 15.

A functional block diagram of the ILAAT math model is shown in Figure 10. A complete description of the equations for each of the block elements shown in Figure 10 can be found in Reference 12.

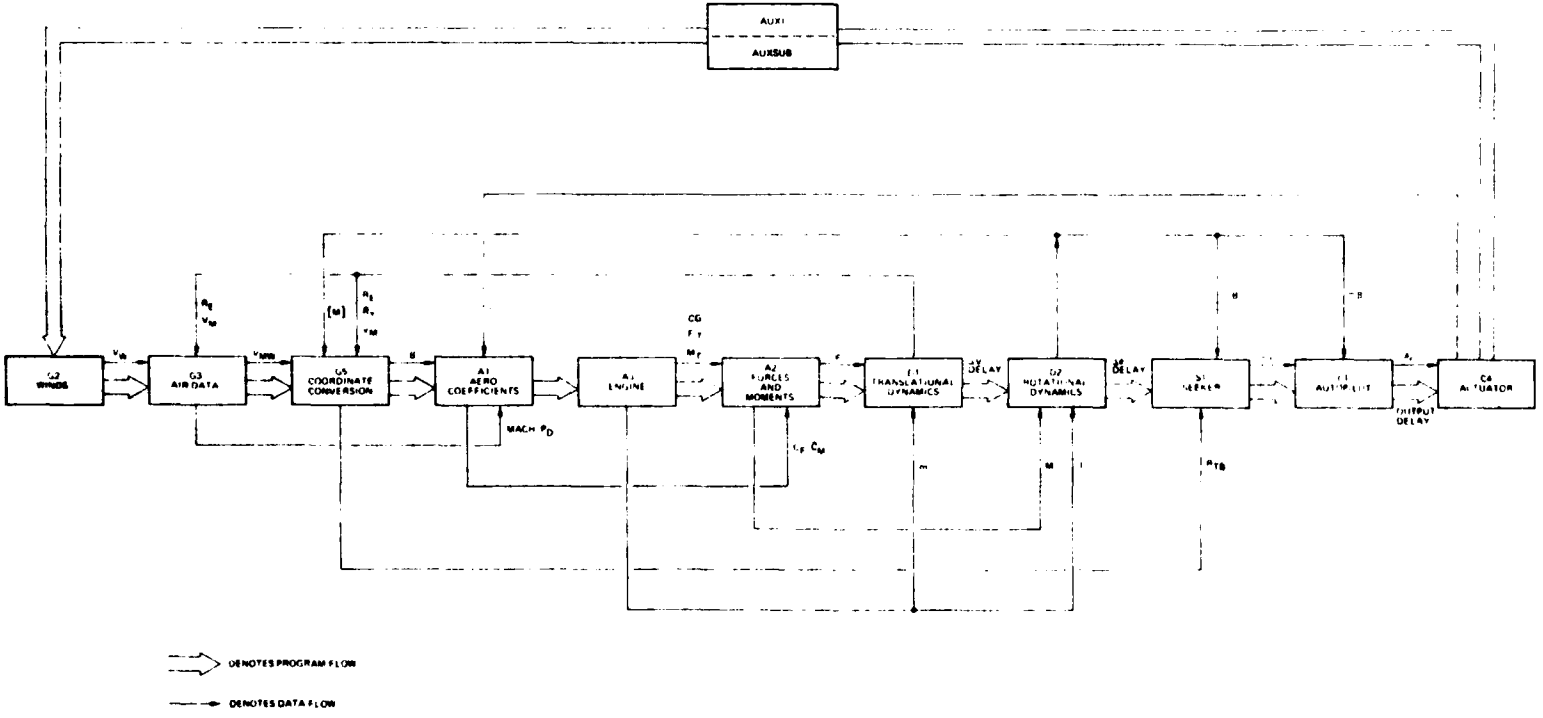


Figure 10. ILAATS Mathematical Model Functional Block Diagram

The ILAAT DAP math model is shown in Figure 11. The autopilot design was obtained from the analog design shown in Figure 12 (Ref. 16), by the application of the matched z-transform to first and second order transfer functions. A complete description of the ILAAT autopilot math model is given in Appendix A and Reference 15.

NOTE: The LCIGS is not part of the ILAAT math model because of its low frequency response characteristics. See Paragraph 4.2.1.

3.3.2 GBU-15

The GBU-15 is an air-to-surface guided bomb which is dropped from an aircraft against fixed ground targets. The GBU missile examined in this study is the planar wing weapon (PWW) configuration shown in Figure 13. A typical PWW trajectory is shown in Figure 14 and consists of three primary flight sequences following separation from the carrying aircraft (Ref. 13). During midcourse, the weapon is controlled in pitch solely to maximize range and does not require target-dependent sensor information. The midcourse sequence begins after separation and continues until transition. During transition, the weapon is steered in yaw using proportional navigation. Angle of attack is maintained in the pitch plane. The weapon goes into the terminal phase when the pitch line-of-sight reaches a predetermined value. The math model for the GBU-15 is similar in structure to the ILAAT model shown in Figure 10 (Ref. 13) and was provided to CSC as GFE. See Reference 17.

The GBU-15 autopilot provides control for all phases of the flight. A mathematical model of the autopilot is shown in Figure 15. A digitization of the continuous autopilot shown in Figure 15 was performed by Hughes Aircraft Company and is discussed in Reference 13.

Note in Figure 15 that the LCIGS feeds information to the autopilot and in effect acts as the autopilot sensor. A simplified mathematical model of the LCIGS gyro and accelerometer subsystems is shown in Figure 16 and 17, respectively.

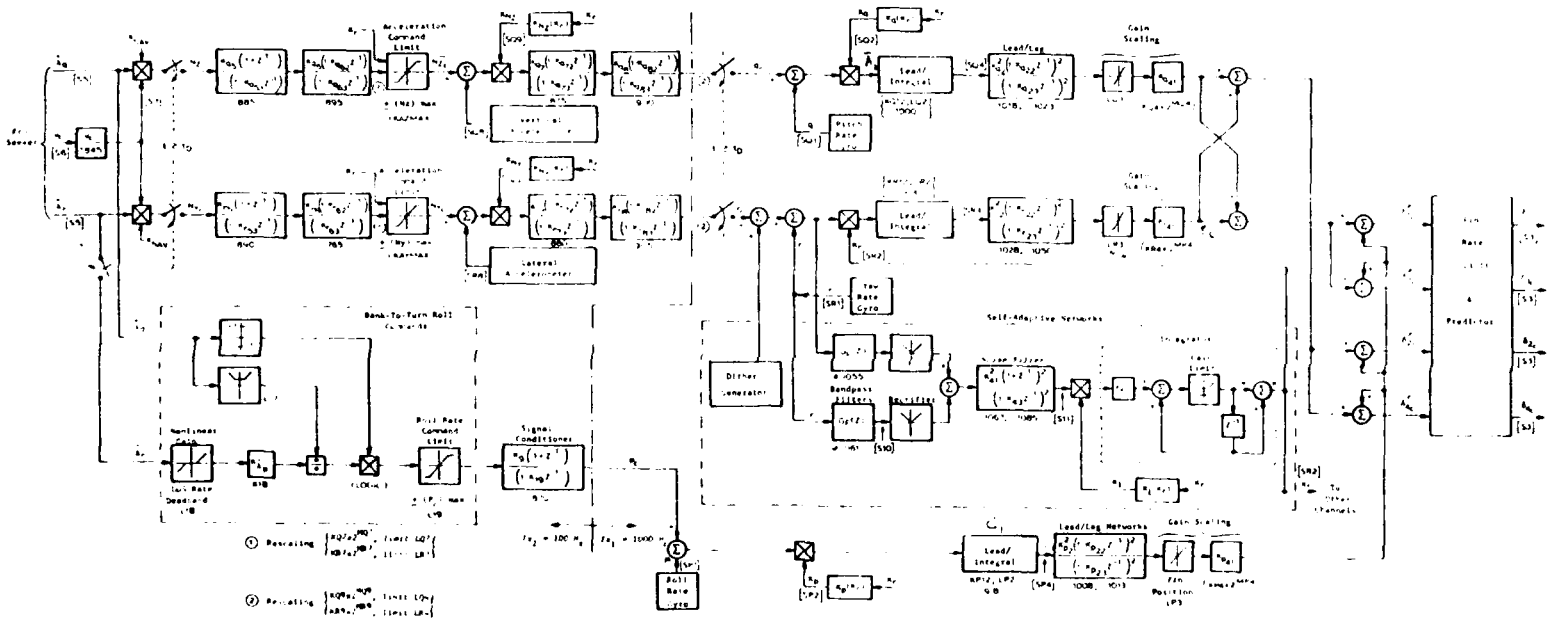


Figure 11. ILAAT Digital Autopilot Mathematical Model

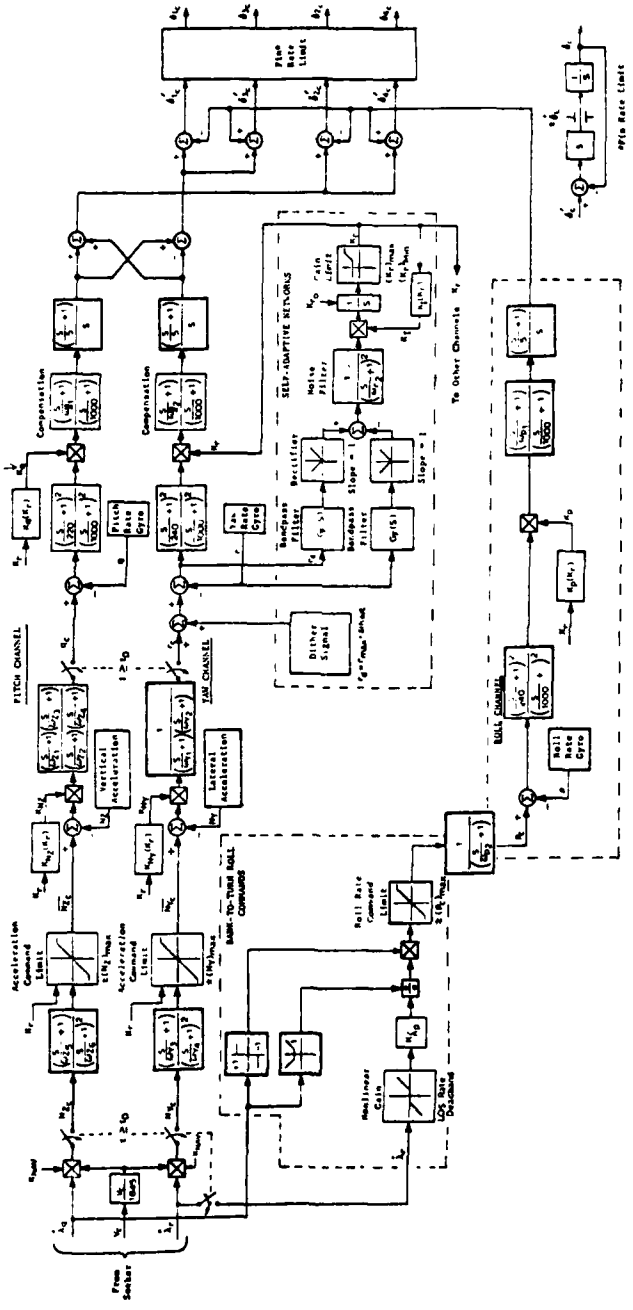


Figure 12. ILAAT Analog Autopilot Mathematical Model

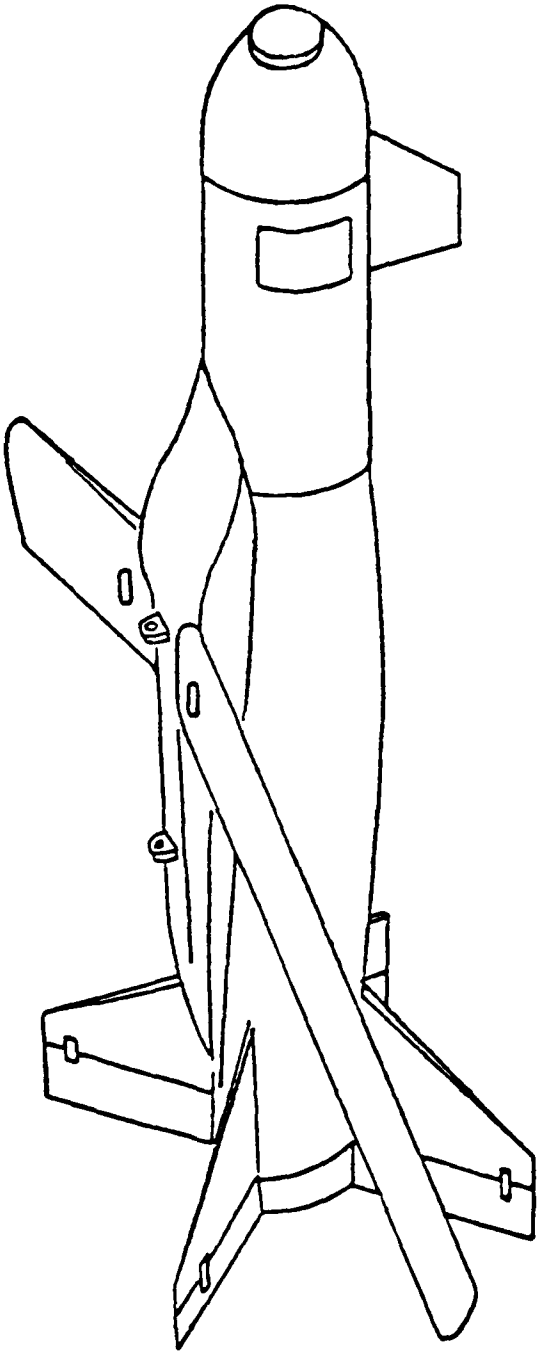


Figure 13. Planar Wing Weapon Version of GBU-15 Air-to-Surface Missile

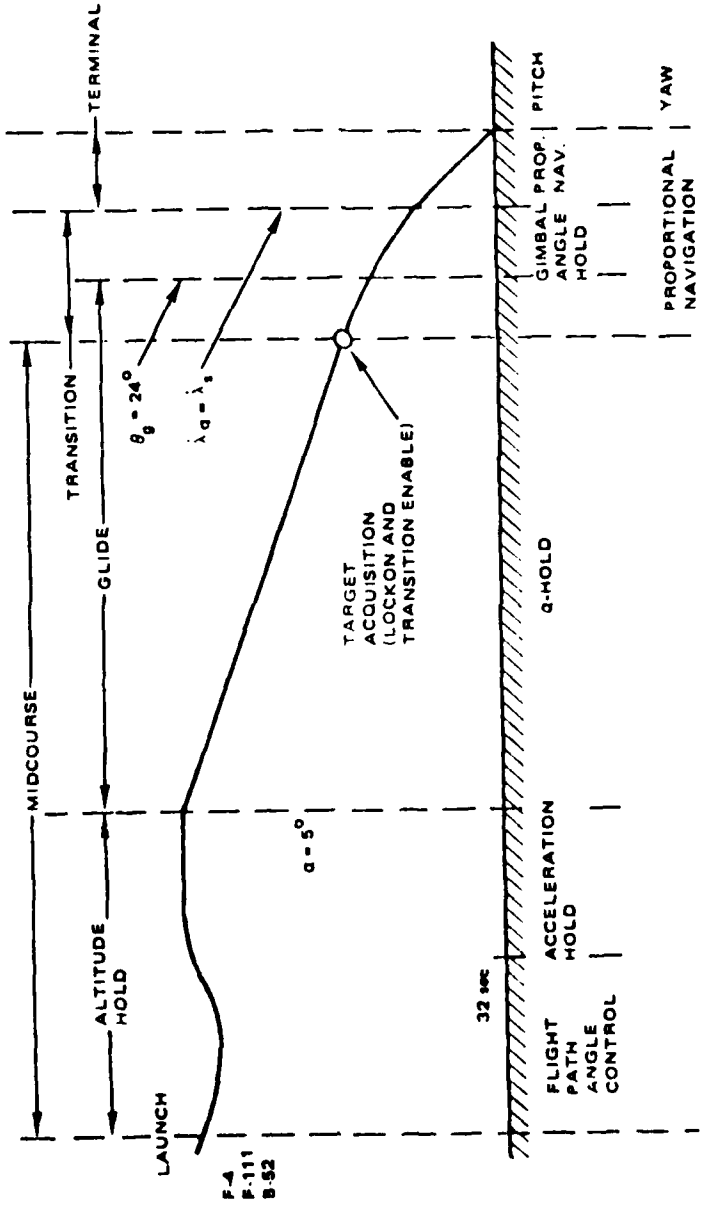


Figure 14. Typical PWW Trajectory

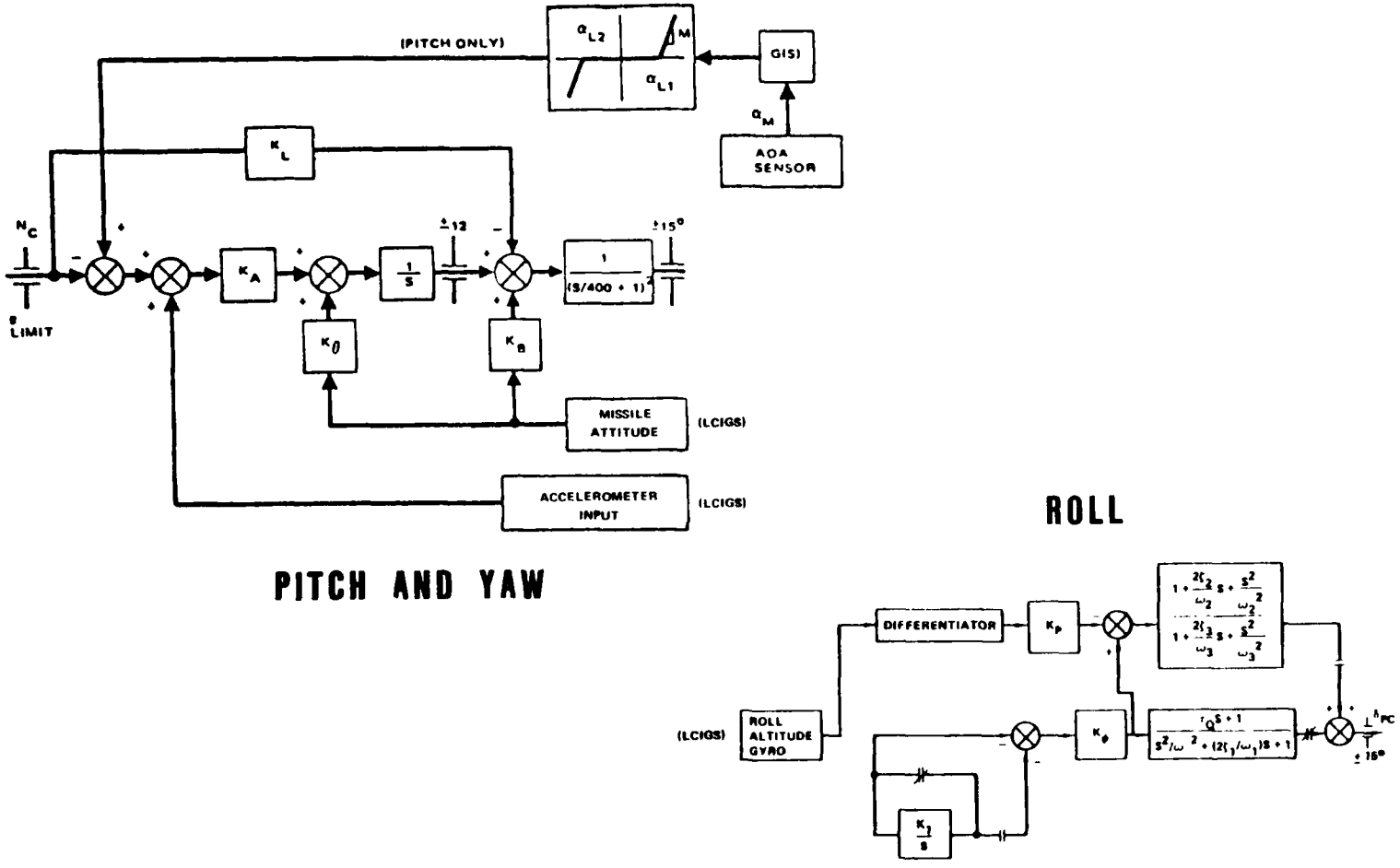
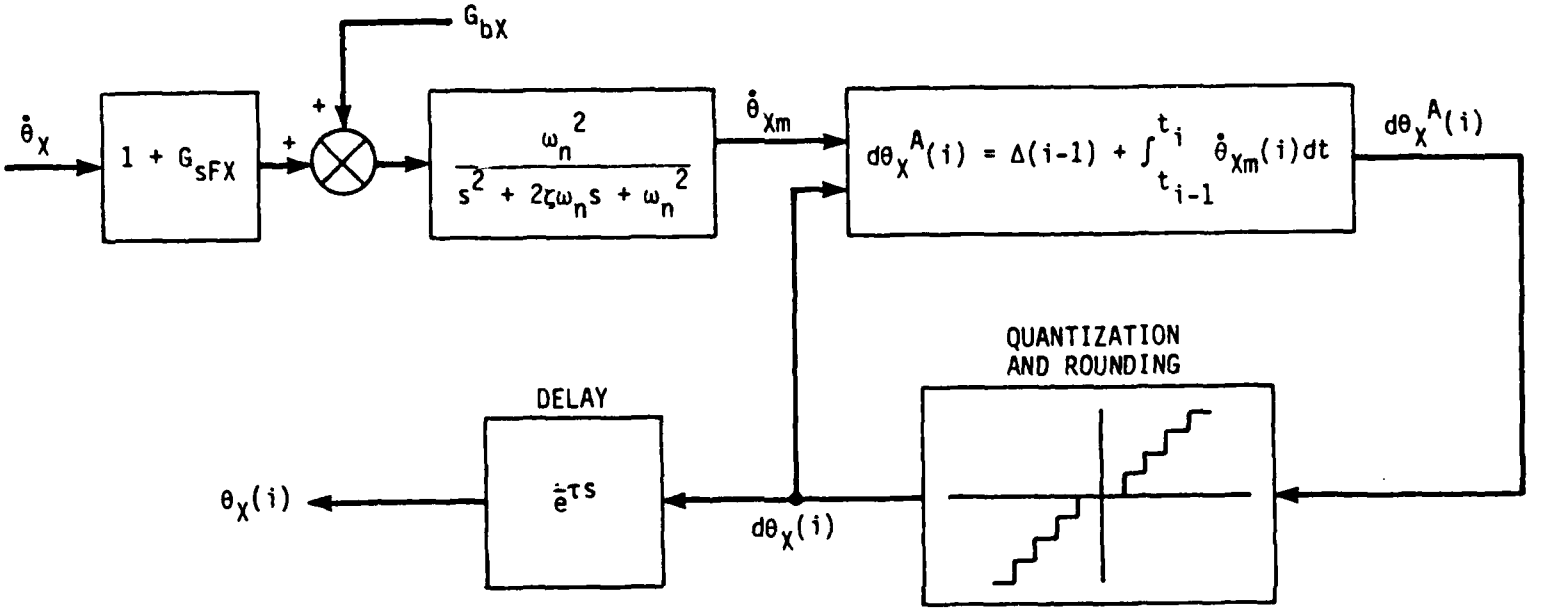


Figure 15. GBU-15 PWW Autopilot Math Model



NOMENCLATURE:

$\dot{\theta}_X$ = SENSED MISSILE TURN RATE

G_{sFX} = X-GYRO SCALE FACTOR ERROR

G_{bX} = X-GYRO BIAS ERROR

$80 \leq \omega_n/2\pi \leq 100$

$0.3 \leq \zeta \leq 0.7$

$\Delta(i-1) = d\theta_X^A(i-1) - d\theta_X(i-1)$: $j=i-1$

$d\theta_X^A(i)$ = i^{th} INCREMENTAL ANGLE PRIOR TO ROUNDING

$d\theta_X(i)$ = i^{th} INCREMENTAL ANGLE AFTER ROUNDING

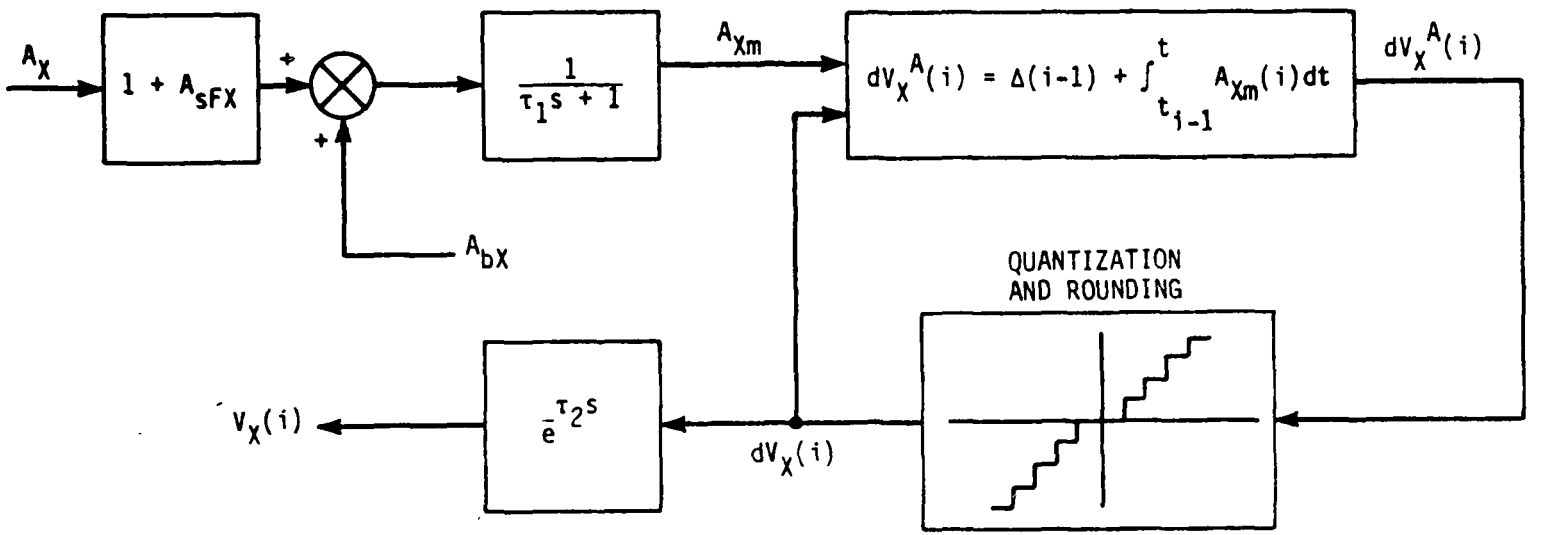
$\dot{\theta}_{Xm}(i)$ = i^{th} MEASURED ANGULAR RATE

$1.38(10^{-3}) \leq \tau \leq 1.48(10^{-3})$ SECONDS

$\theta_X(i)$ = i^{th} INCREMENTAL ANGULAR DISPLACEMENT AROUND THE X-AXIS AFTER DELAY

NOTE: Y AND Z MODELS ARE THE SAME WITH X REPLACED BY Y AND Z

Figure 16. LCIGS Gyro Mathematical Model (Source: Lear Siegler, Inc.)



NOMENCLATURE:

A_X = SENSED MISSILE X-ACCELERATION

A_{sFX} = X-ACCELEROMETER SCALE FACTOR ERROR

A_{bX} = X-ACCELEROMETER BIAS ERROR

$\tau_1 = [(2\pi)(250)]^{-1}$

$1.335(10^{-6}) \leq \tau_2 \leq 1.435(10^{-6})$

$\Delta(i-1) = dV_X^A(i-1) - dV_X(i-1)$

$dV_X^A(i)$ = i^{th} INCREMENTAL VELOCITY PRIOR TO ROUNDING

$dV_X(i)$ = i^{th} INCREMENTAL VELOCITY AFTER ROUNDING

$A_{Xm}(i)$ = i^{th} MEASURED ACCELERATION

$V_X(i)$ = i^{th} INCREMENTAL VELOCITY IN X-DIRECTION AFTER DELAY

NOTE: Y AND Z MODELS ARE THE SAME WITH X REPLACED BY Y AND Z

Figure 17. LCIGS Accelerometer Mathematical Model (Source: Lear Siegler, Inc.)

SECTION IV
MISSILE SYSTEM PERFORMANCE ANALYSIS

4.1 GENERAL

The mathematical models of the ILAAT and GBU-15 missiles, presented in the previous section, are used in this section to evaluate the effect of data latency on missile performance.

Classical stability analysis techniques are used in Paragraph 4.2 which correlate time delay, phase margin, and missile stability.

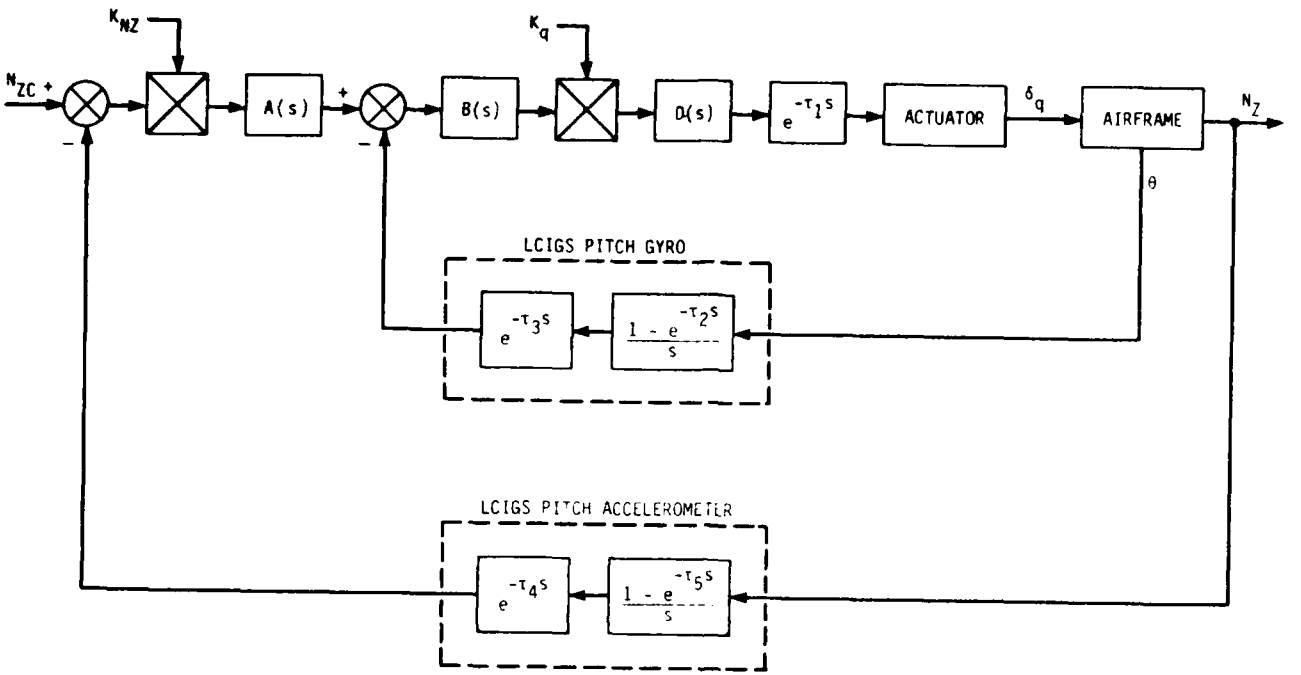
Time domain simulation results of the models presented in Paragraph 3.3 are given in Paragraph 4.3.

4.2 THEORETICAL RESULTS

4.2.1 ILAAT

The nonlinear mathematical model of the ILAAT previously discussed was linearized and simplified for ease of analysis. A block diagram of the ILAAT with pitch plane autopilot is shown in Figure 18. Second order transfer functions were used for the airframe plant. The LCIGS pitch gyro and accelerometer transfer functions were represented by a calculation time delay phase lag and a zero-order hold. A phase lag has been inserted after the D(s) transfer function to simulate the autopilot calculation time delay. The actuator transfer function is assumed to be ideal.

An attempt to solve the characteristic equation with zero calculation time constants yielded semi-infinite positive roots indicating that the system is unstable as configured in Figure 18. It was concluded that the bandwidth of the LCIGS pitch gyro and accelerometer models is not sufficient to allow the system output to follow the input. It was decided that the LCIGS model would not be used with the ILAAT vehicle model in the digital simulation. The system was found to be stable without the LCIGS model.



NOMENCLATURE:

- N_{ZC} = COMMANDED PITCH ACCELERATION
- K_{NZ} = ACCELERATION GAIN (12.0 DEG/SEC/G)
- K_q = PITCH RATE GAIN (5.824)
- τ_1 = AUTOPILOT CALCULATION TIME CONSTANT
- τ_2 = 1/400 SECONDS
- δ_q = PITCH FIN DEFLECTION
- $\dot{\theta}$ = ANGULAR PITCH RATE
- N_Z = PITCH ACCELERATION AT CENTER OF GRAVITY
- τ_3 = LCIGS PITCH GYRO CALCULATION TIME CONSTANT
- τ_4 = LCIGS PITCH ACCELEROMETER TIME CONSTANT

$$A(s) = \frac{\left(\frac{s}{5} + 1\right)\left(\frac{s}{150} + 1\right)}{\left(s + 1\right)\left(\frac{s}{17} + 1\right)}$$

$$B(s) = \frac{\left(\frac{s}{220} + 1\right)^2}{\left(\frac{s}{1000} + 1\right)^2}$$

$$D(s) = \frac{\left(\frac{s}{70} + 1\right)\left(0.2\,s + 1\right)}{\left(\frac{s}{1000} + 1\right)^5}$$

Figure 18. Linearized ILAATS Pitch Plane Mathematical Model

4.2.2 GBU-15

A block diagram of a simplified GBU-15 mathematical model is shown in Figure 19. The math model is highly nonlinear and must be linearized to use classical control theory to analyze stability. A linearized version of Figure 19 is shown in Figure 20. Note in Figure 20 that the LCIGS pitch gyro and accelerometer transfer functions are represented by a calculation time delay phase lag and a zero-order hold. A phase lag has also been inserted after the F(s) transfer function to simulate the autopilot calculation time delay. The actuator transfer function is assumed to be ideal. A block diagram of the airframe transfer function is shown in Figure 21.

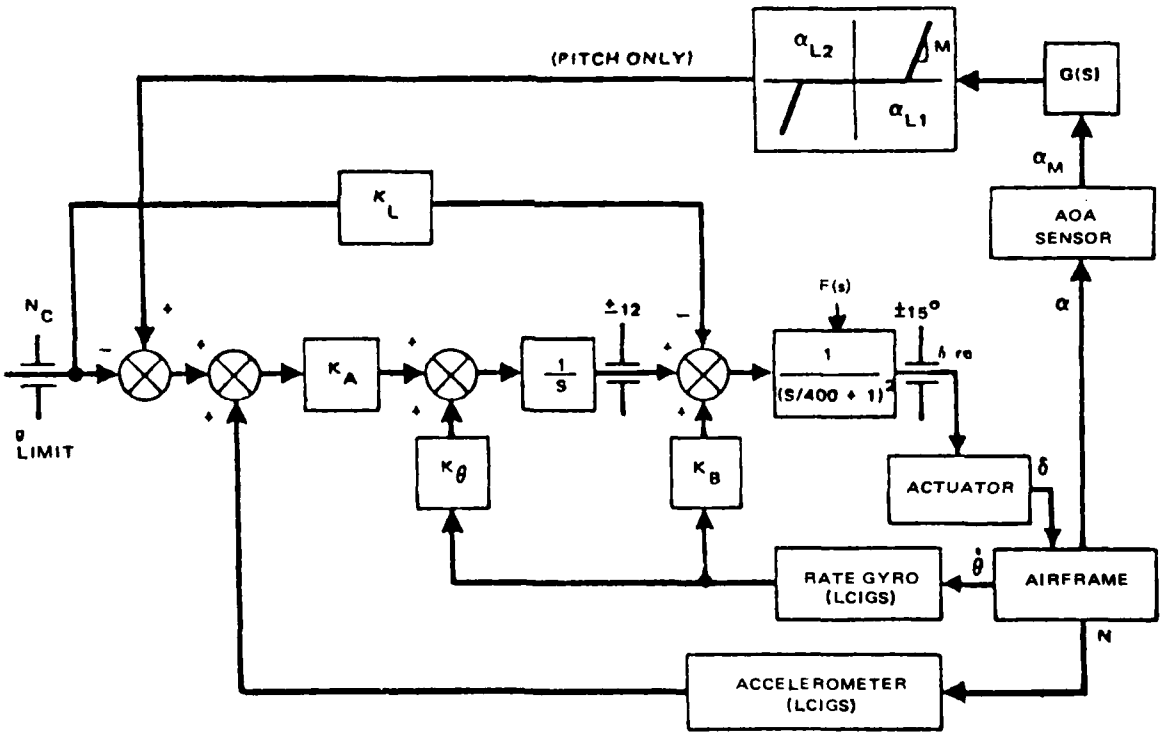
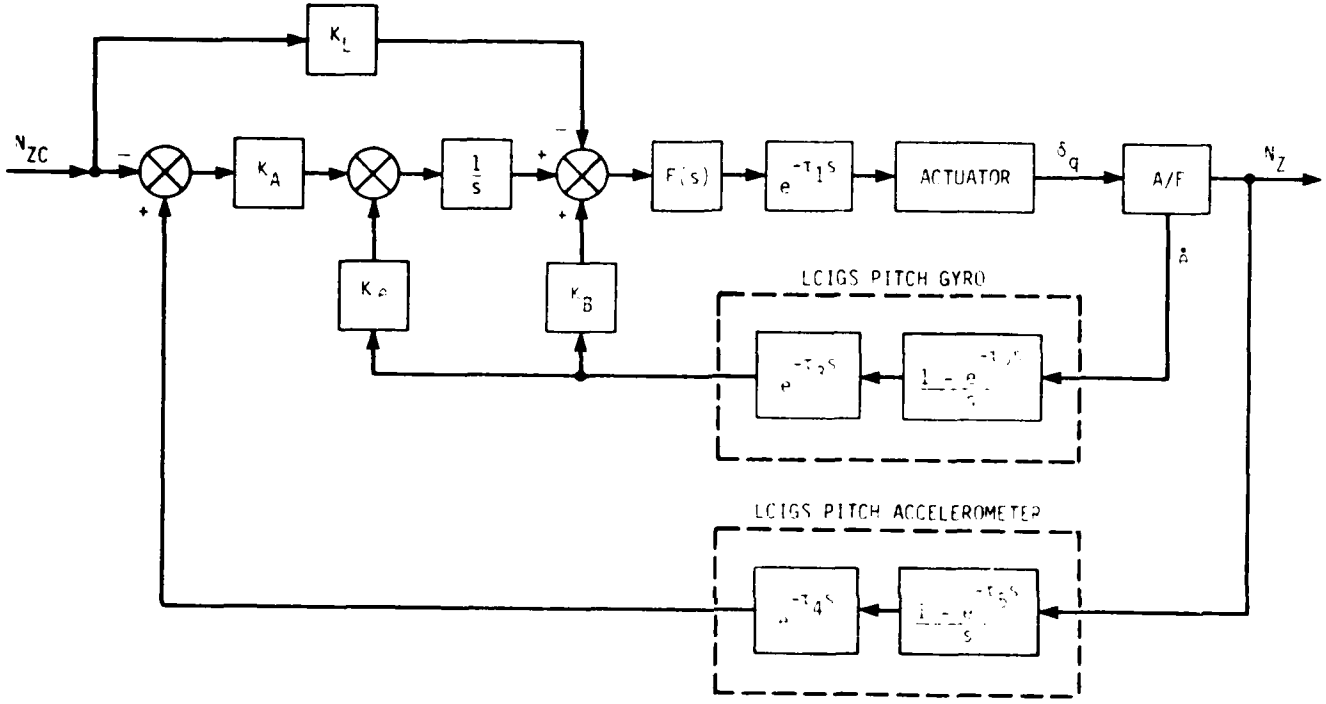


Figure 19. GBU-15 Mathematical Model (Simplified)



NOMENCLATURE (REF. 13)

N_{ZC} = COMMANDED PITCH ACCELERATION

K_A = ACCELERATION GAIN ($3.255(10^{-3})$ DEG/SEC/G

$F(s) = \left[\frac{s}{400} + 1\right]^{-2}$

τ_1 = AUTOPILOT CALCULATION TIME CONSTANT

δ_q = PITCH FIN DEFLECTION

$\dot{\theta}$ = ANGULAR PITCH RATE

N_Z = PITCH ACCELERATION AT CENTER OF GRAVITY

τ_2 = 1/400 SECONDS

τ_3 = LCIGS PITCH GYRO CALCULATION TIME CONSTANT

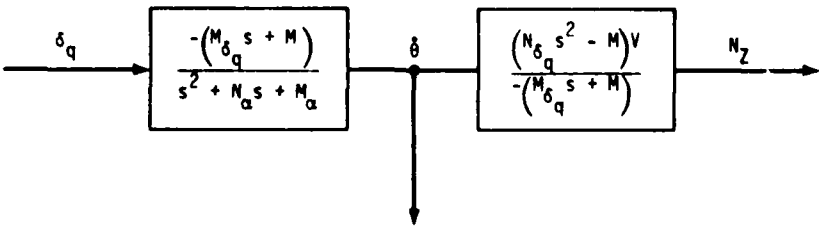
K_B = RATE GAIN (0.25 SEC)

K_θ = ATTITUDE GAIN (1.0)

τ_5 = 1/400 SECONDS

τ_4 = LCIGS PITCH ACCELEROMETER CALCULATION TIME CONSTANT

Figure 20. Linearized GBU-15 Pitch Plane Mathematical Model



NOMENCLATURE:
$M = M_{\delta_q} N_\alpha - M_\alpha N_{\delta_q}$ and $M_{\delta_q} = 21.3$, $N_{\delta_q} = 0.046$, $M_\alpha = 8.9$, $N_\alpha = 0.46$ ARE AERODYNAMIC PITCH MOMENT COEFFICIENTS DEFINED IN REFERENCE 13. V IS THE WEAPON VELOCITY (500 FT/SEC).

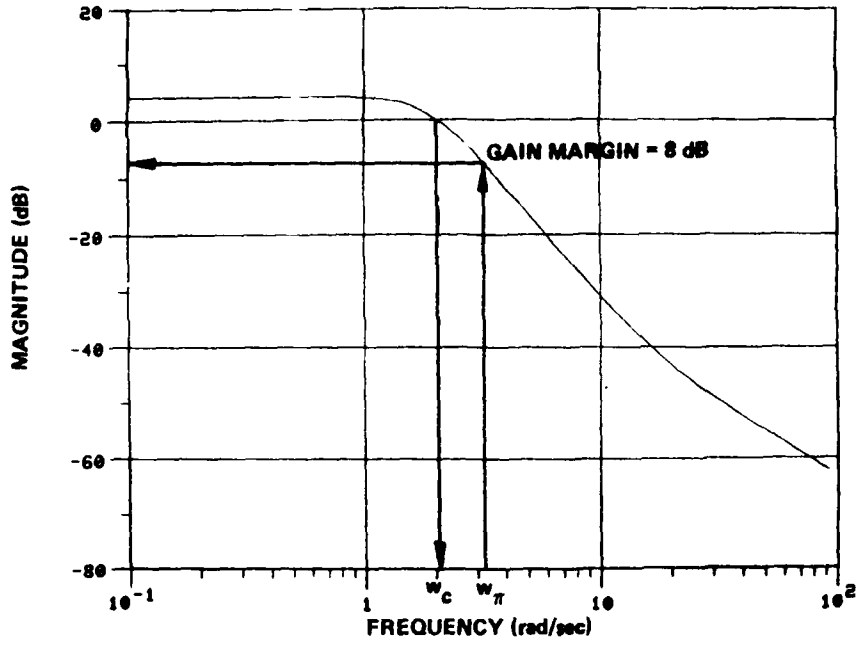
Figure 21. GBU-14 Airframe Transfer Function

A typical Bode plot of the open loop transfer function of Figures 20 and 21 is shown in Figure 22. Stability response in terms of phase margin versus autopilot and LCIGS calculation time delays is shown in Table 6. The phase margin decreased to 44 degrees for LCIGS and autopilot time delays of 0.060 sec each or a total loop delay of 0.12 sec. Note that the system stability is considered to be questionable when the phase margin drops below 45 degrees.

TABLE 6. GBU-15 PHASE MARGIN VERSUS CALCULATION TIME DELAY

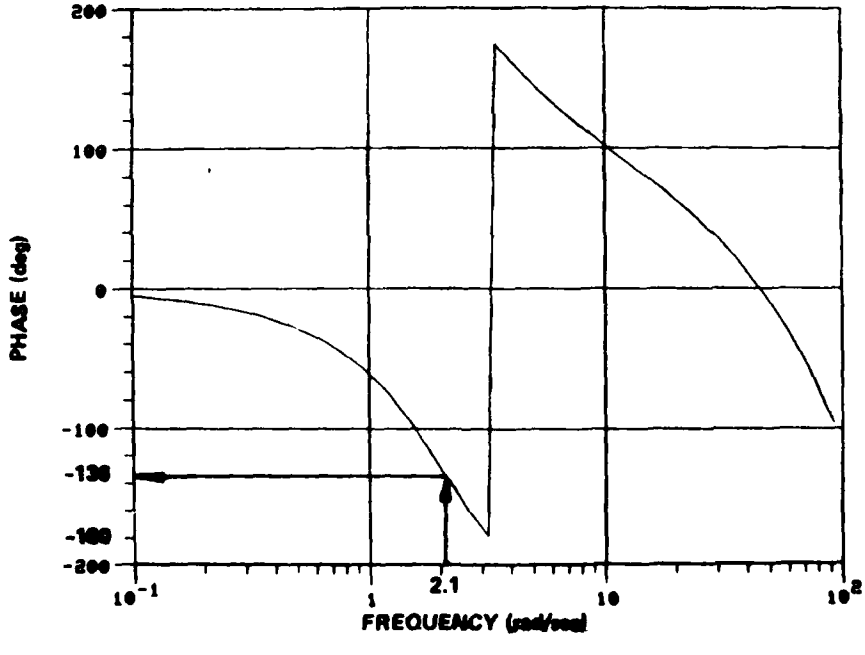
LCIGS TIME DELAY* (SEC x 10^{-3})	AUTOPILOT TIME DELAY (τ_1) (SEC x 10^{-3})	PHASE MARGIN (DEGREES)
0.0	0.0	50.0
1.0	1.0	47.8
5.0	5.0	47.5
10.0	10.0	47.0
20.0	20.0	46.5
30.0	30.0	46.0
40.0	40.0	45.4
50.0	50.0	45.0
60.0	60.0	44.0

*PITCH (τ_3) AND ACCELEROMETER (τ_4) TIME DELAY VALUES



w_π = 3.4 rad/sec

w_c = 2.1 rad/sec



ϕ_m = 180 − 136 = 44°

Figure 22. Typical GBU-15 Bode Plot Set (Autopilot and LCIGS Calculation Time Delay is 0.060 sec Each)

4.3 SIMULATION RESULTS

4.3.1 ILAAT

The ILAAT simulation is a six-degree-of-freedom (6-DOF) modular simulation which was originally built to assess the performance of the Active Laser Seeker (Ref. 12). Modifications to the simulation include the insertion of a delay subroutine and a bank-to-turn (BTT) digital autopilot subroutine. Due to problems in determining correct scale factors for the BTT autopilot (Appendix B), this subroutine could not be used in this analysis. Instead, delays were inserted at the output of the analog autopilot (Figure 12) to simulate the effect of DAP delays. Although LCIGS is not used in ILAATS (Paragraph 3.3.1), delays were inserted at the input of the autopilot subprogram to simulate the delay effects of an "artificial LCIGS".

The results of the simulation are shown in Figures 23 through 28. The missile goes completely unstable with a delay of 0.014 sec at the autopilot and "LCIGS outputs". Since the delays are in series, the total loop time delay is 0.028 sec.

4.3.2 GBU-15

The results of the GBU-15 simulation are presented in this paragraph. The government furnished simulation (Ref. 17) is similar to the model discussed in Paragraph 3.3.2 except that the LCIGS model is not used. The LCIGS math model was coded and inserted into the simulation, but its use caused erratic results in the simulation output. It was therefore decided to run the simulation without the LCIGS but with delay subroutine calls inserted in the roll gyro (ROLLGY) subprogram and in the accelerometer (ACCEL) subprogram. These subroutines perform functions similar to LCIGS and calculate the accelerometer and gyro values which are output to the digital autopilot. A delay subroutine call was also inserted at the output of the autopilot subroutine to simulate calculation time delays.

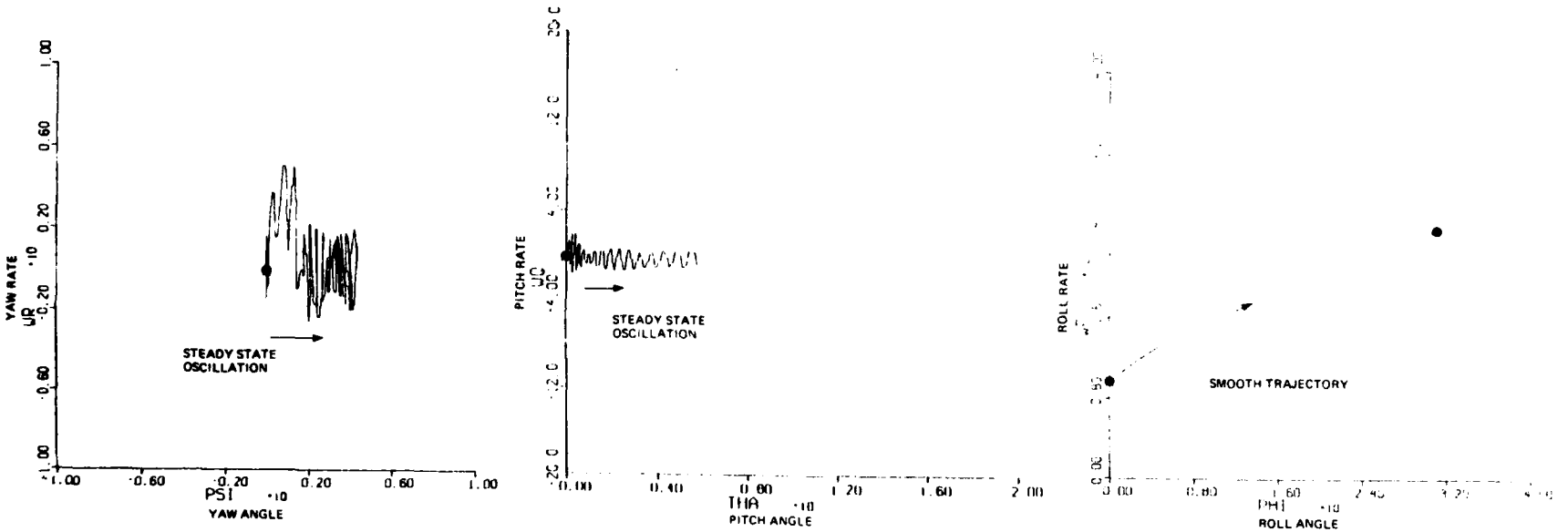


Figure 23. ILAAT Attitude Phase Plane Response with Total Vehicle Loop Time Delay of 0.0 sec

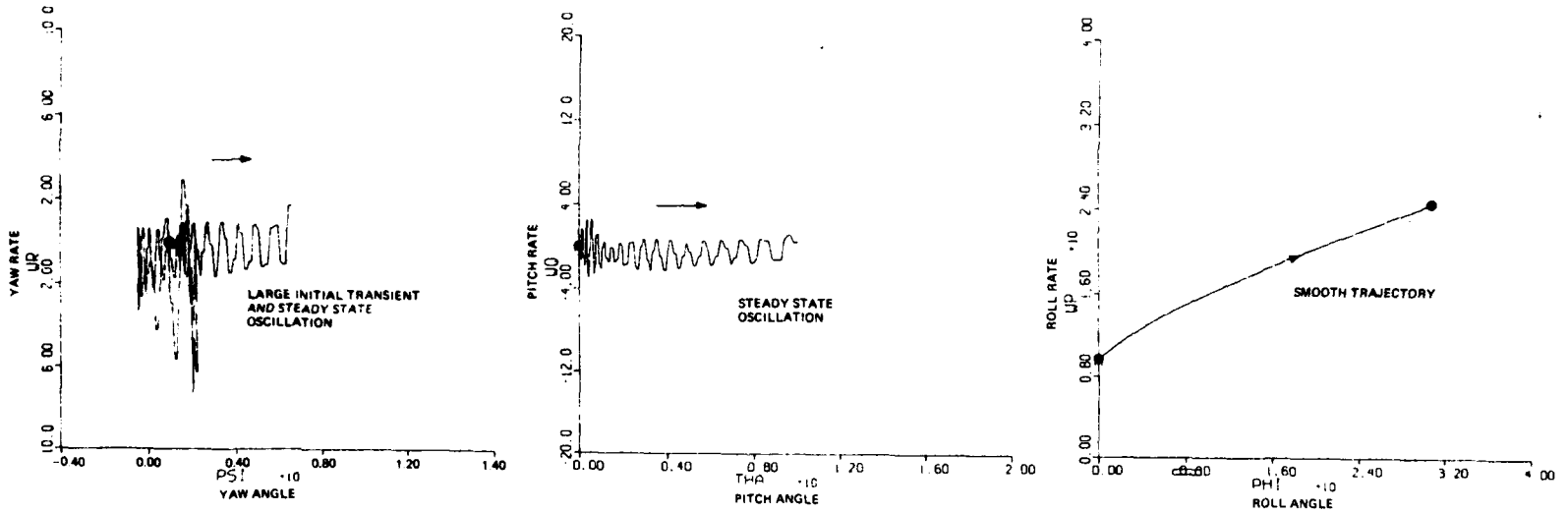


Figure 24. ILAAT Attitude Phase Plane Response with Total Vehicle Loop Time Delay of 0.024 sec

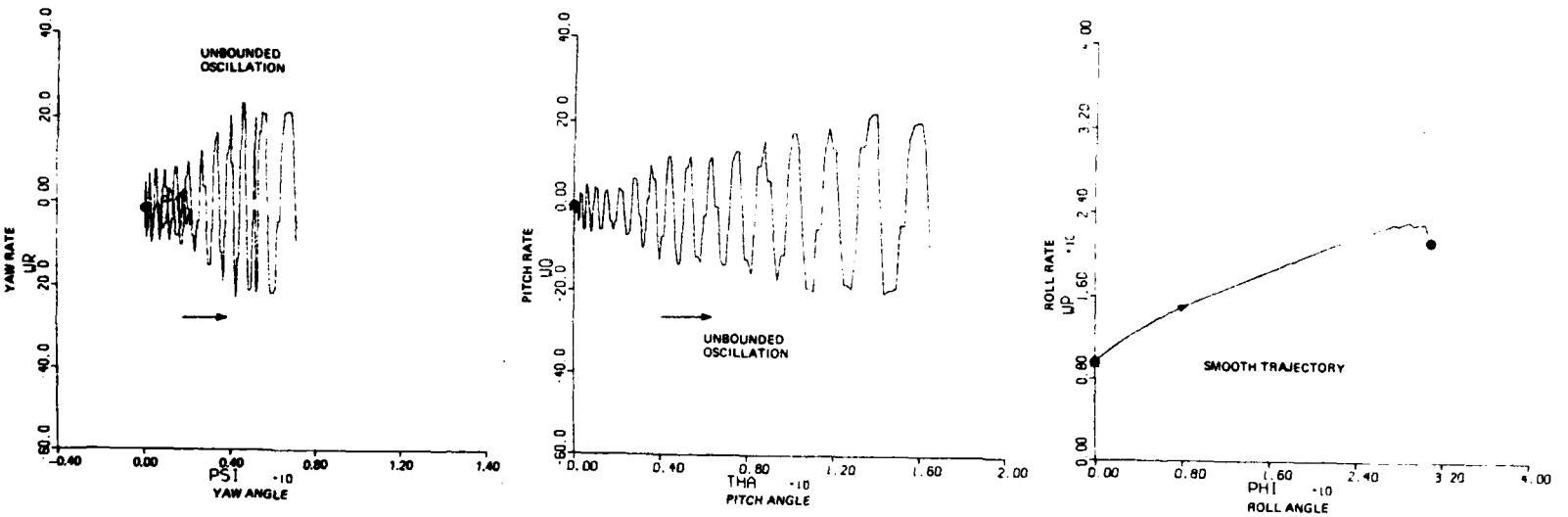


Figure 25. ILAAT Attitude Phase Plane Response with Total Vehicle Loop Time Delay of 0.028 sec

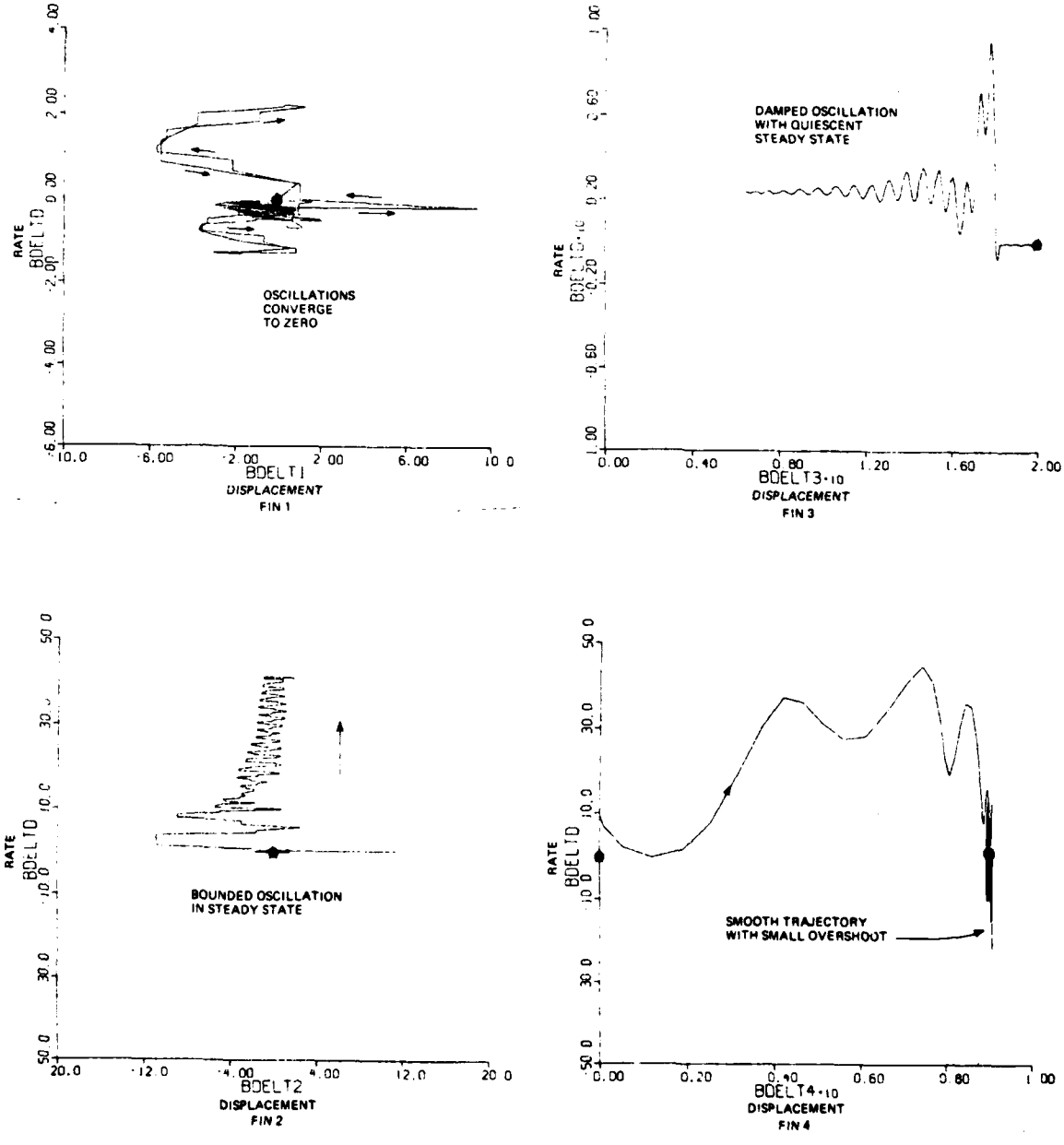


Figure 26. ILAAT Fin Phase Plane Response with Total Vehicle Loop Time Delay of 0.0 sec

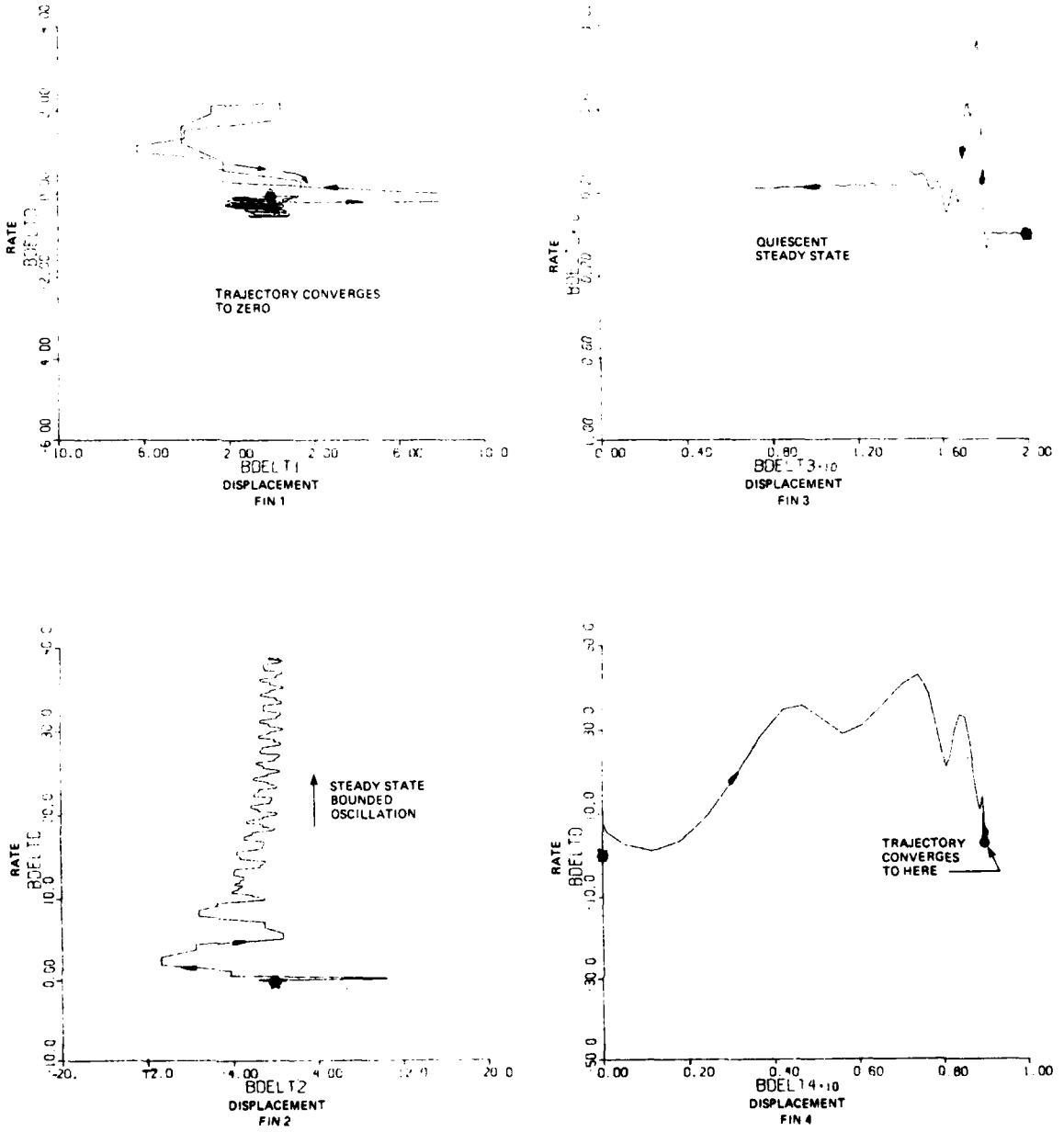


Figure 27. ILAAT Fin Phase Plane Response with Total Vehicle Loop Time Delay of 0.024 sec

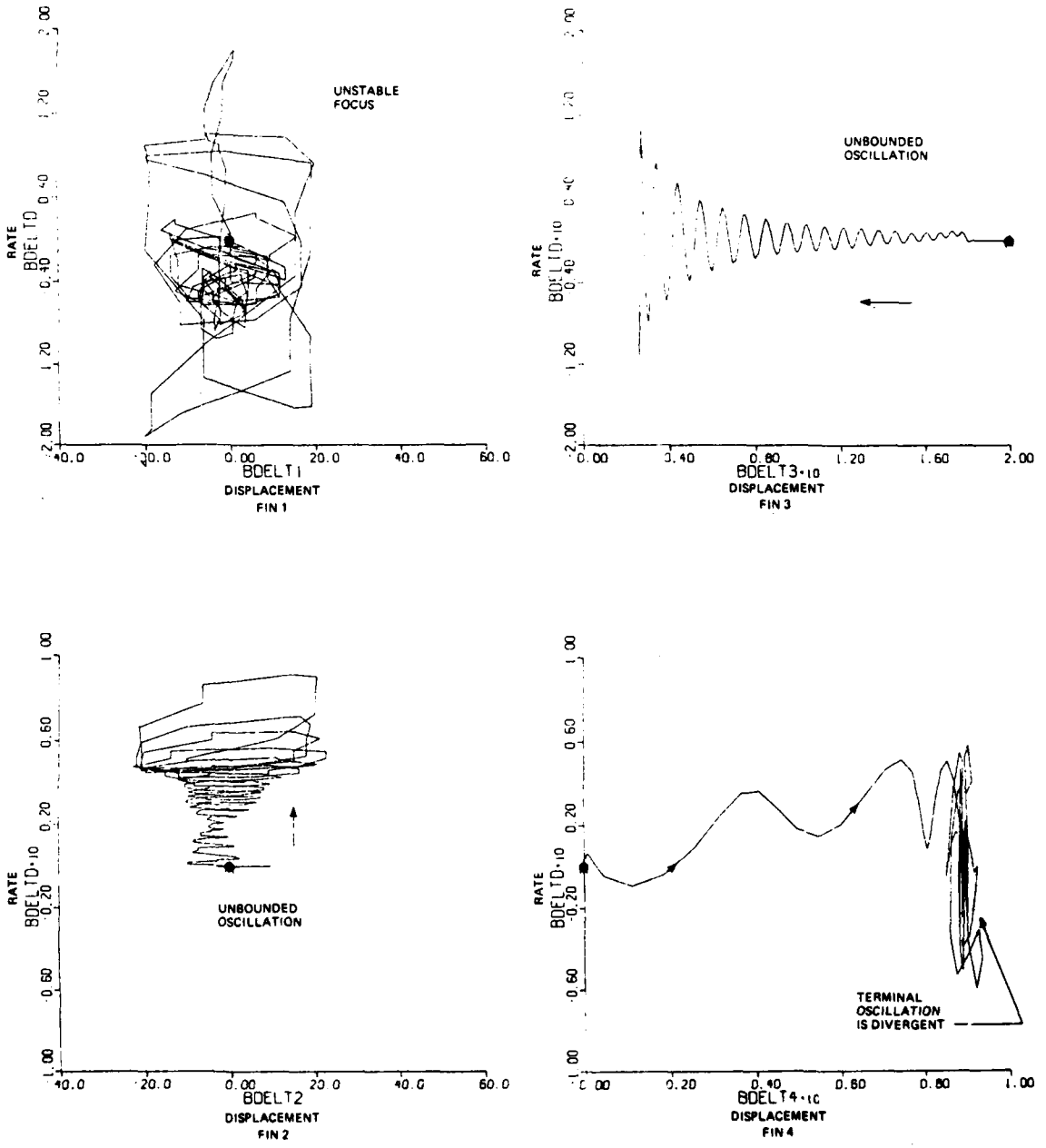


Figure 28. ILAAT Fin Phase Plane Response with Total Vehicle Loop Time Delay of 0.028 sec

Results of the simulation are shown in Figures 29 through 34 (figures show incipient instability). The missile goes unstable with an LCIGS and autopilot delay of 0.15 sec. Since these delays are in series, the total loop time delay is 0.30 sec.

4.4 SUMMARY

Table 7 summarizes the main results of the theoretical and simulation analysis. When using the criteria of 45 degrees as an unsatisfactory stability margin for the linear theoretical results, the GBU-15 has a loop delay of approximately 50 percent of the unstable coupled pitch-roll-yaw nonlinear simulation results. It should be noted that the theoretical results of the GBU-15 are predicated on a linear mathematical model of the system in the pitch plane whereas the six-degree-of-freedom simulation is a highly nonlinear model of the entire missile. Thus the results obtained in Table 8 should be used as an order of magnitude check rather than an absolute value check.

The pitch plane results obtained for the ILAAT were inconclusive and due to time constraints, it was decided not to pursue that analysis further.

TABLE 7. LOOP DELAY COMPARATIVE SUMMARY TABLE
(TIME IN SECONDS)

	ILAAT	GBU-15
THEORETICAL RESULTS (PITCH PLANE)	N/A	0.120
SIMULATION RESULTS (PITCH, YAW, ROLL COUPLED)	0.028	0.300

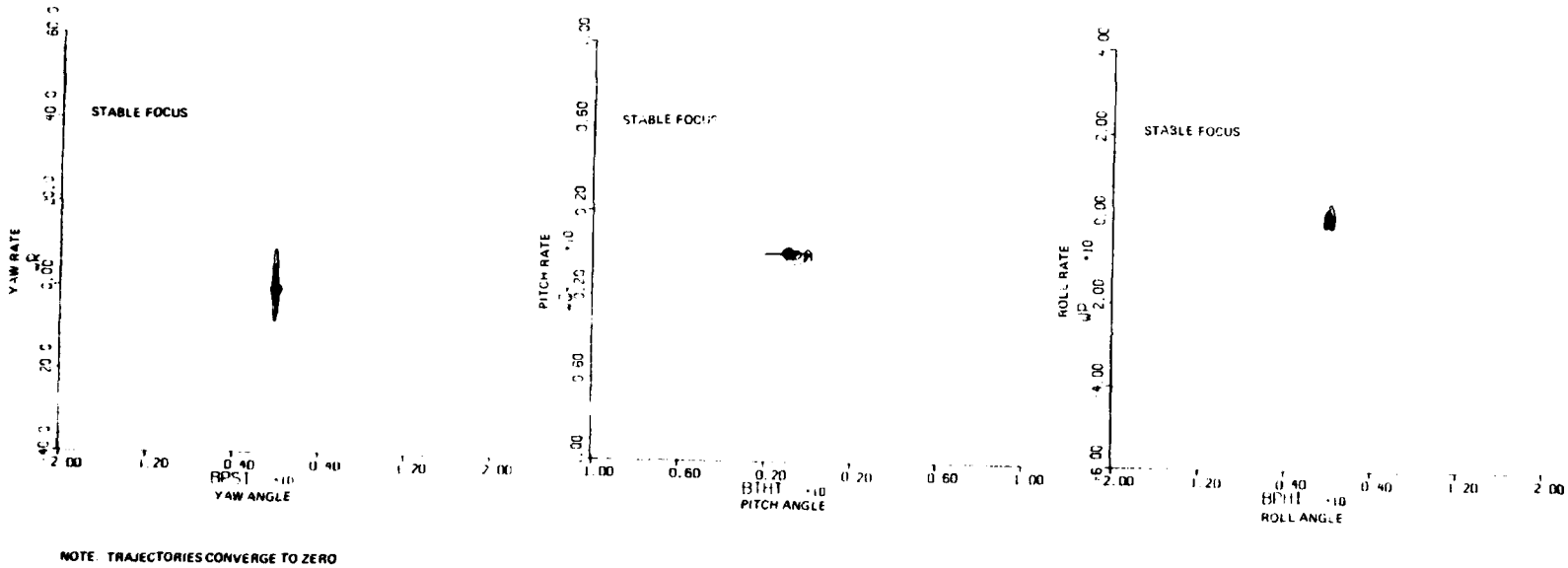


Figure 29. GBU-15 Attitude Phase Plane Response with Total Vehicle Loop Time Delay of 0.0 sec

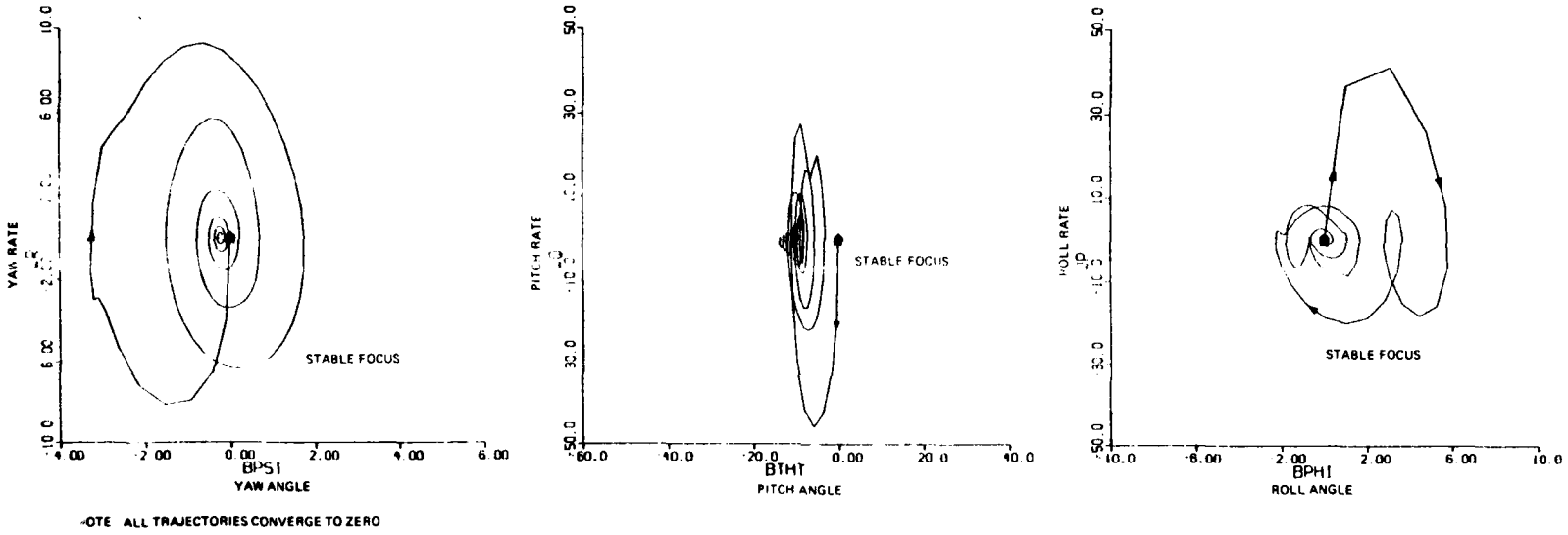


Figure 30. GBU-15 Attitude Phase Plane Response with Total Vehicle Loop Time Delay of 0.20 sec

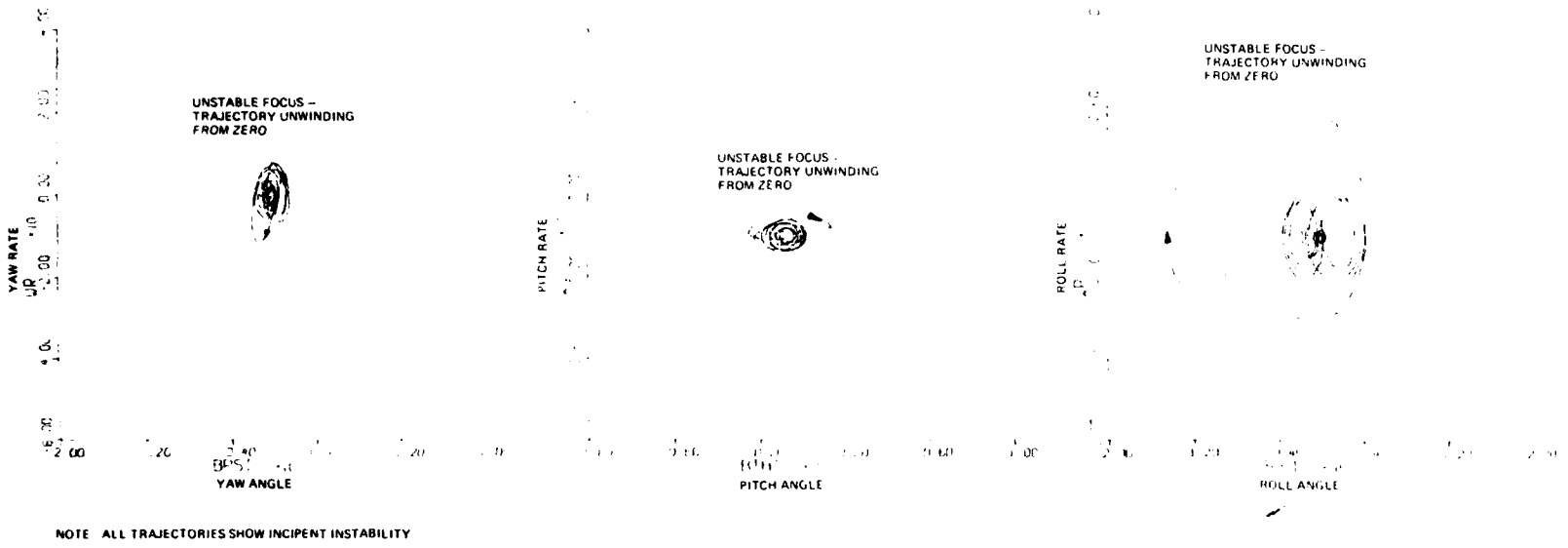


Figure 31. GBU-15 Attitude Phase Plane Response with Total Vehicle Loop Time Delay of 0.300 sec

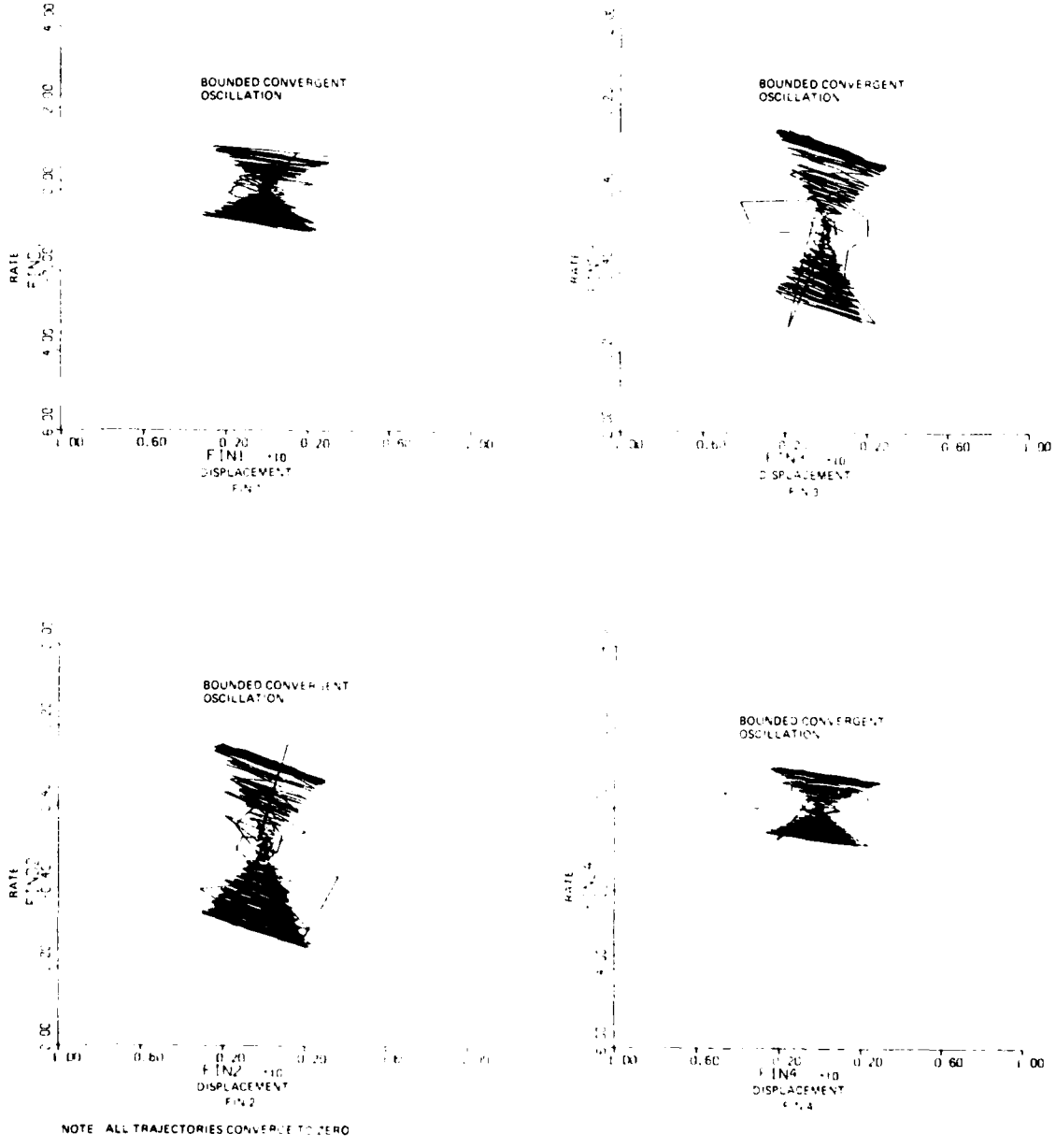


Figure 32. GBU-15 Fin Response with Total Vehicle Loop Time Delay of 0.0 sec

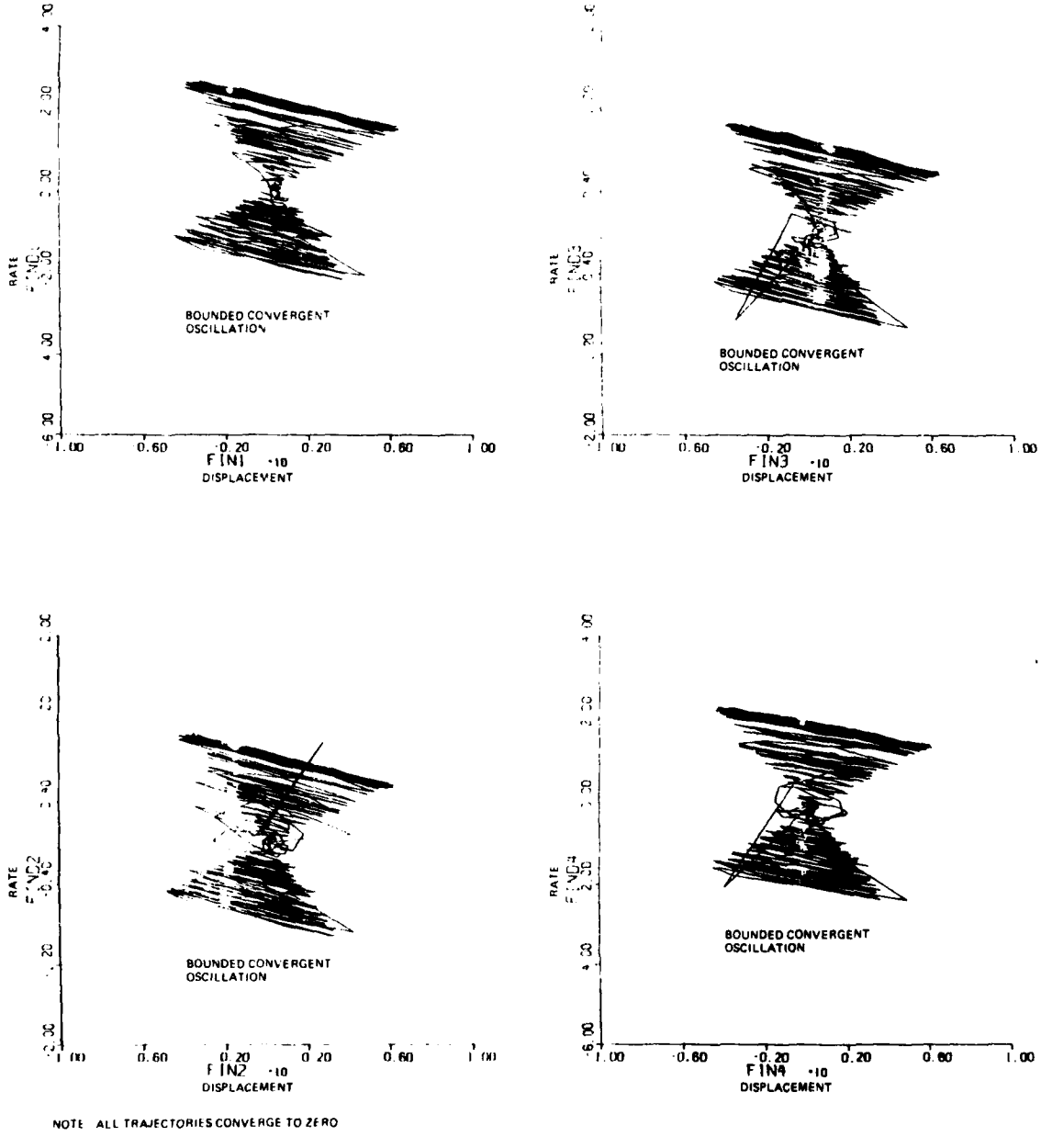


Figure 33. GBU-15 Fin Response with Total Vehicle Loop Time Delay of 0.20 sec

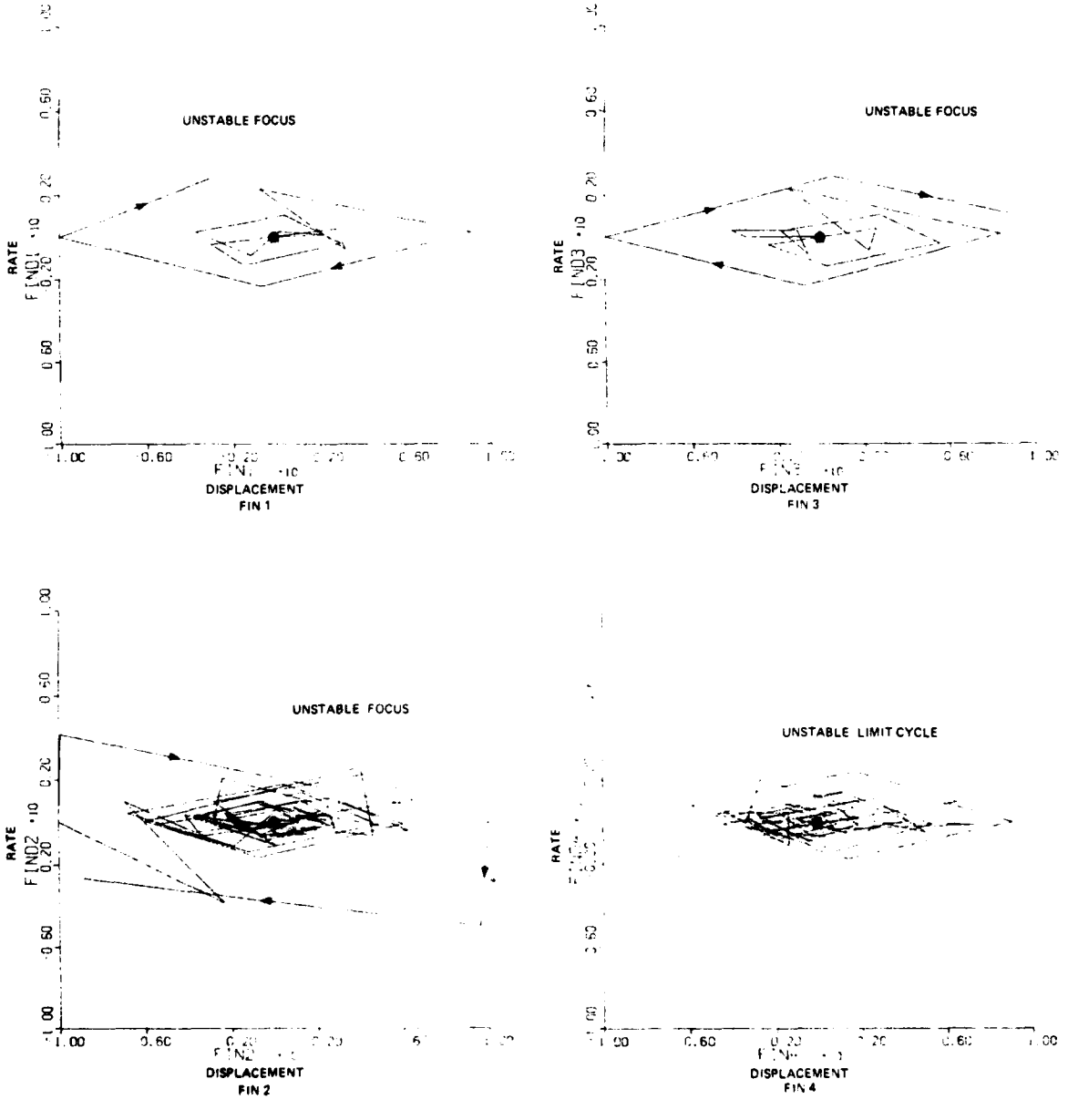


Figure 34. GBU-15 Fin Response with Total Vehicle Loop Time Delay of 0.300 sec

SECTION V
CONCLUSION

As stated in the Introduction, the goals of this study were to (1) examine the DIS latency inherent in interprocessor I/O communication schemes and (2) to obtain quantitative data relating missile performance to time delay. The results of the first part of this study (Section II) confirmed that parallel interfacing of data between DIS modules produces the lowest latency time and that the LCIGS-DAP-FCAS latency which results when all of the main processors are on the bus (including LCIGS and FCAS) is approximately 6 msec for the TERCOM Configuration. This is a very small fraction of the time delay required to drive the missiles studied unstable. See Section III.

The results of the second part of this study showed that the highly maneuverable air-to-air ILAAT missile is approximately ten times more sensitive to phase lag than the GBU-15 air-to-surface missile (Table 6).

APPENDIX A
ILAAT BANK-TO-TURN AUTOPILOT ANALYSIS

A.1 ANALOG STRUCTURE

A block diagram of the ILAAT baseline bank-to-turn (BTT) analog autopilot was shown previously in Figure 12. The flight control system's stability and dynamics are controlled by a self-adaptive network, using the output gain (K_r) to schedule other loop gains and limiters. The yaw rate loop is excited by an externally generated sinusoidal dither signal with amplitude sensed by bandpass filters. The filtered signals are rectified, then differenced to generate an error signal. The error signal is passed through a noise filter which also suppresses dither frequency harmonics. The signal is integrated at a rate which is a function of the adaptive gain K_I to generate the yaw rate loop gain (K_r). A constant yaw rate loop cross-over frequency is thus maintained which is identical to the dither frequency. A limit was placed on the output signal of the adaptive loop integrator to prohibit transients from producing output gains which are outside the permitted maximum and minimum values of K_r.

The pitch and yaw rate loops are used to dampen the aero mode and, together with the roll loop, use lead integral forward loop shaping. This promotes easier scheduling of the outer pitch and yaw acceleration loops and gives the roll loop the ability to attain commanded roll rate values. The roll and pitch rate loop gains are scheduled from K_r and all three rate loops use a 1000 rad/sec pole to generate a fin rate command limit to protect the actuators from velocity saturation commands. The double lead networks in the pitch and yaw rate loops add phase margin at the loop cross-over frequency without significantly decreasing the gain margin. All three rate loops also employ a 20-degree fin command limit.

The pitch and yaw acceleration loops are utilized for steering and provide a positive method to implement a missile acceleration control limiter. The adaptive gain K_r is used to schedule the acceleration loop gains and command limiter stops.

Steering is accomplished by generating roll command rates proportional to the yaw LOS rate ($\dot{\lambda}_r$) which rolls the missile until $\dot{\lambda}_r$ is zeroed. The sign of the roll command is determined by the sign of the product of pitch LOS rate ($\dot{\lambda}_q$) with the yaw LOS rate $\dot{\lambda}_r$. This rolls the missile pitch axis into the maneuvering plane through the smallest roll angle. A deadband in $\dot{\lambda}_r$ is provided to eliminate unnecessary roll commands due to seeker biases and cross-coupling. The roll homing loop gain, $K_{\dot{\lambda}_P}$ is divided by the pitch LOS rate, $\dot{\lambda}_q$, to provide adequate response at low $\dot{\lambda}_q$ and stability at high $\dot{\lambda}_q$. A roll rate command limit was mechanized to reduce large roll rate commands which limit the required range of the roll rate gyro and which also provide a method to adjust time-to-roll to 90 degrees.

A.2 DIGITAL STRUCTURE

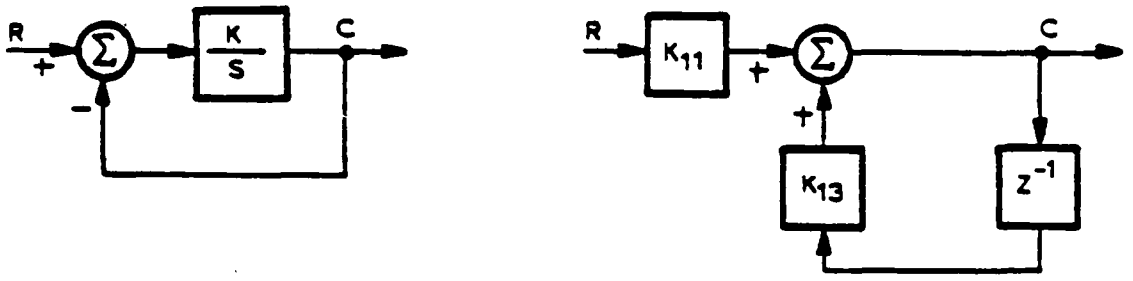
The ILAAT BTT digital autopilot (DAP) model was shown previously in Figure 11. Z-transform techniques were used to convert the dynamical elements of the analog autopilot, previously discussed, to digital filters (Ref. 15). Digitization included lead integrators in the pitch, yaw and roll channels, the dither signal generator, two bi-l filters, the noise filter, and the adaptive gain integrator in the self-adaptive network.

The matched z-transform method was used to convert all analog filters to their digital equivalent. Trapezoidal integration was employed to obtain the z-plane equivalents of the integrators used in the analog version.

In the matched z-transform method of filter design all poles ($s = -p_i$) and zeros ($s = -u_i$) of the analog prototype filter are transformed into digital poles and zeros located at $z = e^{-pi^T}$

and $z = e^{-ui^T}$, respectively, where T is the sampling period. A constant multiplier can be chosen to adjust the overall gain of the resulting filter.

An example of the matched z-transform application to a first-order lag is shown in Figure A-1.



$$G(S) = \frac{C}{R}(S) = \frac{1}{S/\omega_0 + 1}$$

where:

$$K = \omega_0$$

analog form

$$G(Z) = \frac{C(Z)}{R(Z)} = \frac{K_{11}}{(1 - K_{13} Z^{-1})}$$

where:

$$K_{11} = (1 - K_{13})$$

$$K_{13} = e^{-\omega_0 T}$$

digital form

Figure A-1. Analog and Digital (Z-Transform) Implementations of a First-Order Lag

Pertinent parameters in the DAP model, which are discussed fully in Reference 15, include sample rates, word length, filter coefficients and gain scaling.

A.3 ANALYSIS RESULTS

The conversion of DAP filters from the s-plane to the z-plane by the matched z-transform method was checked with regard to poles, zeros, and dc gain. The analog autopilot data (Ref. 15) was used as a baseline. The following agreements and discrepancies were found. The filter coefficient values listed in Reference 15 are found to be correct with the exception of those for the dither frequency bandfilters, numbers 1005 and 1061; the lead/integral

filters, numbers 918, 1000, and 1004; and the dither signal generator, numbers 910 and 014. A dc gain check (z = 1) was performed on all filters of the digital version which correspond to those filters of the analog version which have unity dc gain. Some discrepancies were found between the two versions which could be resolved only by making assumptions regarding table entry values.

The filters labeled compensation in the pitch, yaw, and roll channels immediately prior to the lead/integral filters in the analog version have no counterpart in the digital version. No explanation could be found in Reference 15 for this discrepancy.

Special consideration was given to the two bandpass filters in the self-adaptive networks. In References 15 and 16, the inference is that these bandpass filters should be timed to the dither frequency, w_d. This was found to be the case in the analog version but not the digital version. Discrepancies were also found in the nonlinear gains of BTT roll commands of the analog and digital versions.

Due to the previously mentioned discrepancies, it is not possible to match the outputs of the analog and digital autopilots for similar inputs. Thus the analog autopilot was used as the ILAAT DAP.

APPENDIX B
DIS BUS TRAFFIC MODEL

The baseline bus traffic model is used to assess the effects of transient delays of the DIS shown in Figure B-1. The model consists of 10 processors, 6 of which access the bus directly. The 6 on-bus processors are the Sensor Seeker (SSKR), Navigation Aiding Management (NAM), Guidance and Navigation (GAN), Inertial Navigation and Reference (INR), Digital Autopilot (DAP), and Supervisor (SUP) with stores management.

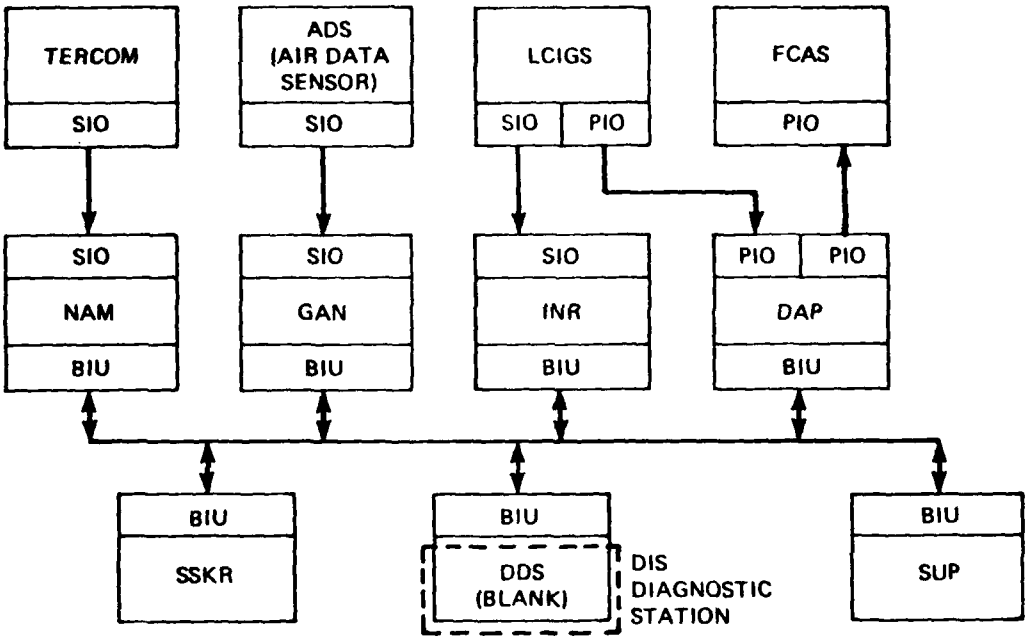


Figure B-1. Bus Traffic Simulator Model (Baseline)

The nonbus processors include the Terrain Contour Matching (TERCOM) Subsystem, Air Data Sensor (ADS), Low Cost Inertial Guidance Subsystem (LCIGS), and Flight Control Actuation Subsystem (FCAS). In the baseline case, the TERCOM and ADS processors are converted to the on-bus NAM and GAN processors, respectively, via a serial input/output (SIO) connection. The LCIGS connects to the INR using a SIO interface and to the DAP using a parallel input/output (PIO) interface. The FCAS is connected to the DAP via a PIO interface interconnection.

It should be noted that TERCOM configuration was used in this study as a worst case message traffic generator causing the longest expected latency times. The total message traffic load for the DIS processors is shown in Table B-1.

BTS attempts to model the DISMUX bus round robin passing protocol as closely as possible. When transmitting signals via DISMUX bus, each processor must wait its turn in the RRPP cycle which is a variable depending on the number of processors and the frequency of message traffic on the bus.

If a particular processor has a message to transmit, a message is prepared and placed on the bus. Each time that a message passes over the bus, the RRPP timing changes. If a particular processor has no message to transmit, an EOT is placed on the bus when the BIO gains access to it.

Several variations of the baseline BTS processor configurations are shown in Figure 8. An important variation of the baseline bus traffic model places both the LCIGS and FCAS on the bus via a BIU interface. These two additional processors cause additional bus waits and asynchronous lags as shown previously in Table 5 (Case E).

See Figure 1 in Volume II for additional details of the BTS simulation.

TABLE B-1. TYPICAL DIS BUS MESSAGE TRAFFIC PROFILE (BASELINE) (TERCOM CONFIGURATION)

SENDING PROCESSOR	RECEIVING PROCESSOR	MESSAGE	NUMBER WORDS XMIT	MESSAGE FREQ. (Hz)	MESSAGE PRIORITY LEVEL
SSKR (NO. 1) ON BUS	GAN	LOS & LOS RATE	4	10	1
	GAN	POSITION	3	1	2
	SUP	STATUS	1	1	3
NAM (NO. 2) ON BUS	GAN	POSITION	3	1	1
	SUP	STATUS	1	1	2
GAN (NO. 3) ON BUS	NAM	ALTITUDE (BAROMETER)	1	10	1
	NAM	ANGLE OF ATTACK	1	10	2
	NAM	TIME, POSITION	4	10	3
	DAP	STEERING DATA	3	10	4
	DAP	CROSS TRACK ERROR	3	1	5
	INR	REFERENCE FRAME RATE	3	10	6
	INR	FILTER STATES	12	0.20	7
	INR	POSITION UPDATES	3	0.25	8
	SUP	STATUS	1	5	9
DAP (NO. 5) ON BUS	FCAS	ACTUATOR COMMANDS	3	200	1
	NAM	RADAR ALTIMETER READING	1	10	2
	GAN	RADAR ALTIMETER READING	1	10	3
	SUP	STATUS	1	5	4
INR (NO. 4) ON BUS	NAM	POSITION & VELOCITY	6	100	1
	DAP	TIME	1	1	2
	GAN	TIME, VELOCITY	5	10	3
	DAP	BANK ANGLE	1	10	4
	GAN	AXIAL ACCELERATION	1	10	5
	GAN	GYRO DATA	3	1	6
	GAN	BODY TO NAVIGATION FRAME TRANSF.	18	1	7
	GAN	COMPENSATED GYRO OUTPUTS	6	1	8
	GAN	BODY TO NAVIGATION FRAME DATA	3	5	9
	GAN	POSITION	3	0.25	10
	GAN	GRAVITATIONAL DATA	1	1.0	11
	GAN	EARTH ROTATION DATA	2	1.0	12
	GAN	RADIUS VECTOR IN INERTIAL SPACE	2	1	13
	GAN	ERROR DATA	6	1	14
	GAN	ACCELERATION DATA	3	1	15
	GAN	VELOCITY DATA	3	1	16
	SUP	STATUS	1	5.0	17
SUP (NO. 6) ON BUS	GAN	TIME, POSITION, VELOCITY	7	1	1

NOTE: THE ABOVE NUMBERS ARE ESTIMATES AND MAY NOT PRECISELY REFLECT AN ACTUAL DIS TERCOM CONFIGURATION.

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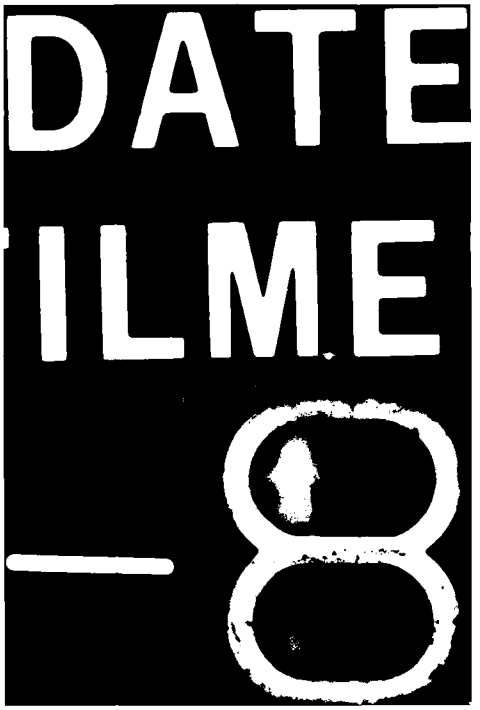
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